Full-Duplex Wireless: Algorithms and Rate Improvement Bounds for Integrated Circuit Implementations

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ABSTRACT

Full-duplex (FD) communication can substantially improve spectrum efficiency in wireless networks. Designing higher layer algorithms (e.g., for power control and scheduling) tailored for FD requires taking into account the special characteristics of the physical layer. In particular, the characteristics of recently introduced integrated circuit (IC) implementations required for mobile devices pose unique challenges. Thus, we describe some of our recent results in the area of antenna and analog/RF cancellation. Then, we overview our corresponding results regarding rate gains and algorithm design when considering these IC-based FD implementations. Finally, we discuss cross-layered open problems.

CCS Concepts

•**Networks** → **Wireless local area networks;** *Network performance analysis;* •**Hardware** → *Wireless devices; Radio frequency and wireless circuits;*

Keywords

Rate improvement; analog and digital cancellation; RFIC

1. INTRODUCTION

Existing wireless systems are half-duplex (HD), where the separation of the node's transmitted and received signals in either frequency or time causes inefficient utilization of limited wireless resources. An emerging technology that can substantially improve spectrum utilization through simultaneous transmission and reception on the same frequency channel is FD wireless communication.

While the concept of FD communication sounds quite simple, in practice it is hindered by numerous challenges (for a comprehensive overview see [10] and references therein). In particular, in many wireless systems, such as Wi-Fi and LTE, the transmitted self-interference (SI) signal is billions of times stronger than the useful signal at the receiver, requiring extremely accurate SI cancellation (SIC).

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Recent work [2, 4, 6] established the feasibility of SIC and FD wireless using laboratory bench-top equipment and off-the-shelf components. The goal in [2, 4, 6] was to bring FD capability to base stations and infrastructure, where the cost and form factor constraints are relatively relaxed. However, the designs from [2, 4, 6] are generally not suitable for low-cost, small form factor, and/or integrated implementations, such as those required for mobile devices. More recently, our work [14–16] and [11, 13] demonstrated SIC and FD operation within CMOS ICs. Yet, utilizing the benefits of these small form factor implementations requires a careful redesign of both the physical and MAC layers.

Therefore, within the "Full-duplex wireless: from Integrated Circuits to Networks" (FlexICoN) project [1], we take a holistic cross-disciplinary approach that spans the domain between physical layer IC design and MAC layer algorithm design. In this paper, we describe some of the recent results obtained within this project, discuss the cross-layer aspects, and highlight outstanding challenges.

In particular, in Section 2 we discuss the challenges associated with SI isolation and cancellation in the antenna and analog/RF domains. We focus on the fundamental challenges associated with an integrated FD radio implementation in CMOS and describe our recent implementations of a CMOS non-reciprocal passive circulator and IC-based RF SI cancellers. Then, in Section 3 we discuss the integration of the RF SI cancellers within a transceiver that includes adaptive tuning mechanisms and digital SIC algorithms. We also discuss SIC modeling aspects that are essential for the design of MAC layer algorithms.

In Section 4, we describe analytical results that characterize achievable rate improvements when considering IC-based FD receiver models. Moreover, we discuss resource allocation algorithms for uplink and downlink power and rate assignment. These algorithms were designed based on realistic transceiver models and can serve as building blocks for future MAC protocols. Finally, we discuss open problems associated with integrated FD transceivers, in MAC protocol design for Wi-Fi and small cell networks. We also highlight challenges in experimental evaluation of networks that include IC-based FD transceivers.

2. INTEGRATED FD TRANSCEIVERS

SI isolation and cancellation in the antenna and analog/RF domains prior to digital SIC are crucial for practical FD implementations with realistic receiver and analog-to-digital converter (ADC) dynamic range requirements. Existing FD demonstrations rely on bulky off-the-shelf antenna inter-

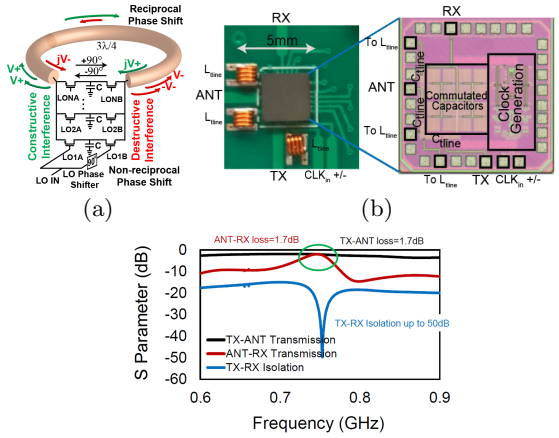


Figure 1: Passive non-magnetic CMOS circulator: (a) concept, (b) 65 nm CMOS implementation, and (c) S-parameters measurement results.

faces (such as non-reciprocal ferrite circulators) and discrete-component-based analog/RF SI cancellers [2,4,6]. However, these antenna interfaces and analog/RF cancellers are not suitable for compact and low-cost integrated-circuit implementations. There are several fundamental challenges associated with an integrated FD radio implementation in CMOS, and we describe them in more detail in the following.

2.1 Antenna Interface

Various antenna interfaces have been reported for FD systems, such as antenna pairs [5], electrical-balance duplexers [12], and circulators. Among them, shared-antenna interfaces (such as electrical-balance duplexers and circulators) are preferable due to channel reciprocity and smaller form factor. Furthermore, reciprocal interfaces such as electrical-balance duplexers suffer from a theoretical 3 dB (practically more) loss; hence more than half of the signal power is lost right at the antenna interface.

Circulators can potentially offer a low-loss, small form factor antenna interface with high transmitter-receiver (TX-RX) isolation. However, commercial circulators are built using ferrite materials and are bulky, expensive, and cannot be integrated on a CMOS platform.

In [9, 16] we conceived, designed, and fabricated the first CMOS non-magnetic non-reciprocal passive circulator, which uses time-variance to break Lorentz reciprocity and mimic the effect of ferrite materials. *This first CMOS passive non-magnetic circulator simultaneously achieves low loss in both directions, high isolation between TX and RX, small form factor, and high linearity for TX signals.* The concept, implementation, and measurement results of the proposed non-magnetic passive circulator are shown in Fig. 1.

2.2 Compact Self-Interference Canceller

One of the fundamental challenges associated with SIC at RF is the cancellation bandwidth due to the frequency selectivity of the antenna interface. A conventional RFIC canceller that we implemented in [14] has a programmable but frequency-flat magnitude and phase response. Thus, the canceller from [14] can only emulate the antenna interface isolation at a single frequency point, resulting in a narrowband SIC (Fig. 2(c)). Wideband SIC at RF based on

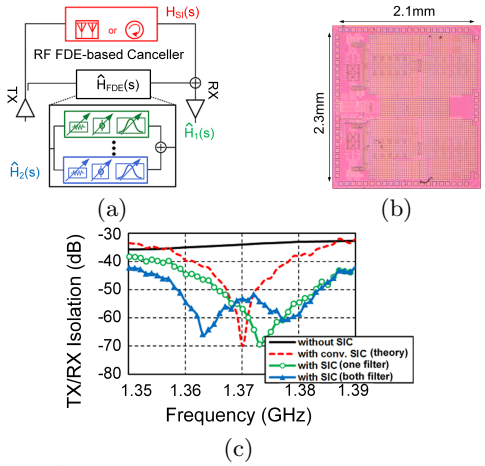


Figure 2: An integrated SIC FD radio receiver with frequency-domain equalization in the RF domain: (a) concept, (b) 65 nm CMOS implementation, and (c) SIC measurement results.

time-domain equalization was reported using multiple on-PCB transmission-line delays and variable attenuators [2]. However, generation of nanosecond-scale true time delay on silicon is extremely challenging due to the required transmission line length and the lossy nature of the silicon substrate.

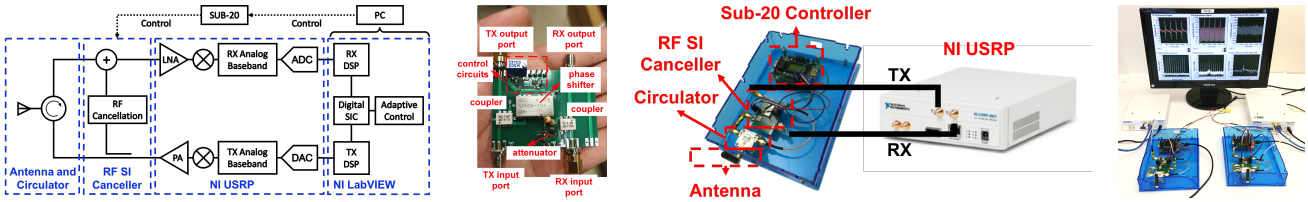
In [15], *we demonstrated integrated SIC in the RF domain using a concept called frequency-domain equalization (FDE).* The FDE technique employs multiple RF bandpass filters (BPFs) with independent control of their magnitude, phase, frequency, and quality factor to emulate the SI channel in different frequency sub-bands. The realization of FDE in the RF domain is accomplished by leveraging modern ultra-scaled CMOS technology – with transistors that are able to be efficiently switched at high frequencies, high-quality factor RF BPFs can be realized based on linear periodically time varying (LPTV) circuits. The concept, implementation, and measurement results of the reported FDE-based FD radio receiver are depicted in Fig. 2.

3. ANALOG AND DIGITAL SIC ALGORITHMS

To experimentally evaluate the conventional and FDE-based cancellers from Section 2.2, we prototyped FD transceivers using custom-designed discrete-component-based RF SI cancellers that emulate their integrated counterparts and National Instruments (NI) Universal Software Radio Peripherals (USRPs). For the conventional canceller, we implemented an adaptive tuning mechanism in [3], while for the FDE-based one, this is a subject of ongoing work (see Section 3.1). To support high levels of SIC, we also implemented an adaptive digital SIC algorithm, described in Section 3.2.

The implemented FD transceiver consists of an antenna, a ferrite circulator, a custom-designed RF SI canceller, and an NI USRP, as illustrated in Figs. 3(a) and 3(c). Fig. 3(a) shows the diagram of an FD transceiver, in which an RF SI canceller (depicted in Fig. 3(b)) taps a reference signal at the output of the power amplifier (PA) and performs SIC at the input of the low-noise amplifier (LNA) at the RX side. Figs. 3(c) and 3(d) show the implementation of an FD transceiver and an FD wireless link that we presented in [3].

3.1 Adaptive Analog/RF SIC Algorithms



(a) (b) (c) (d)

Figure 3: (a) Block diagram of the FD transceiver prototype, (b) the 0.8 GHz to 1.3 GHz frequency-flat amplitude and phase-based (conventional) RF SI canceller, (c) an FD transceiver composed of an antenna, a circulator, a custom-designed RF SI canceller, and an NI USRP, and (d) an FD wireless link that we presented in [3].

In this section, we discuss the adaptive analog/RF SIC algorithms for the two cancellers described in Section 2.2. The adaptive SIC mechanism is simpler to implement for the conventional canceller, at the cost of providing a narrowband SIC, which we demonstrated in [3]. For a more broadband FDE-based canceller, the problem of adaptive RF SIC is more challenging, due to the higher number of configuration parameters and is a subject of our ongoing research.

3.1.1 *Conventional RF SI Canceller*

In [3], the implemented conventional RF SI canceller depicted in Fig. 3(b) emulates the behavior of the RFIC canceller that we presented in [14]. The transfer function (TF) of the canceller can be modeled as $H = A \cdot \exp(-j\phi)$, in which A and ϕ are the frequency-flat configuration parameters of amplitude and phase that need to be tuned to match that of the antenna interface at the center frequency. As mentioned earlier, *this canceller can only emulate the circulator isolation at a single frequency point, resulting in a narrowband SIC* as shown by the red dashed curve in Fig. 2(c). Assuming that the antenna interface has flat amplitude response and linear phase response (constant group delay), it is possible to obtain a closed-form expression for the conventional canceller's residual SIC. We derived such a model in [7] and demonstrated its accuracy via measurements.

Theoretically, only two measurements with different (A, ϕ) settings are needed in order to find the optimal (A, ϕ). However, in practice, the gain at the RF front-end of the USRP is unknown, which complicates the estimation of the amplitude and phase that the canceller should mimic. Thus, in [3], we implemented the adaptive RF SIC mechanism using four measurement points for the three unknowns (A, ϕ, and the USRP gain) and a phase ambiguity to compute an initial configuration, followed by a local tuning to search for the optimal (A, ϕ).

3.1.2 *FDE-based RF SI Canceller*

In our ongoing work, we have been implementing a discrete-component-based canceller that emulates the behavior of the RFIC FDE-based canceller described in Section 2.2 and presented in [15]. As shown in Fig. 2(a), multiple reconfigurable RF BPFs are included in the canceller that channelize the desired signal bandwidth. The TF of the i^{th} path is:

$$\hat{H}_i(j\omega) = \frac{A_i \exp(-j\phi_i)}{1 - jQ_i \frac{\omega_i}{\omega}(1 - \omega^2/\omega_i^2)},$$

where $\omega_i = 1/\sqrt{L_i C_i}$ is the center frequency, $Q_i = \frac{R||R_{p,i}}{\omega_i L_i}$ represents the quality factor, and A_i and ϕ_i are the magnitude and phase settings of the i^{th} BPF, respectively. Thus, an RF canceller with reconfigurable 2^{nd} order RF BPFs features *four degrees of freedom* (A_i, ϕ_i, Q_i, and ω_i) per BPF and *enables the replication of not just the magnitude and phase of the antenna interface isolation at a frequency point, but also the slope of the magnitude and the slope of the phase (or group delay)*. Fig. 2(c) shows the simulated resultant SIC using the wideband FDE-based SI canceller presented in [15] (green and blue curves, for cancellers with one BPF and two BPFs, respectively), compared to the conventional canceller from [14] (red dashed curve).

We remark that although the FDE-based RF SI canceller achieves significantly wider cancellation bandwidth, its tuning is more challenging than for the conventional canceller, since each reconfigurable RF BPF has four parameters to be configured. Moreover, *as the number of BPFs used in the canceller grows, higher bandwidth can be obtained but, on the other hand, the canceller configuration problem becomes more complex*. We are, however, optimistic about the existence of an efficient algorithm for this problem, and are currently working on its design and implementation.

3.2 Digital SIC

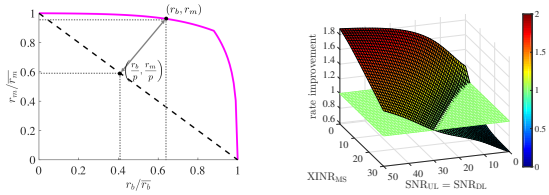
The residual SI after isolation and cancellation in the antenna and RF domains is further suppressed in the digital domain. To cancel both the main SI and the intermodulation distortion generated on the SI, the digital SI canceller is modeled as a truncated Volterra series and is implemented based on a non-linear tapped delay line. Specifically, the discrete-time SI canceller output, y_n, can be written as a function of the current and past TX digital baseband signals, x_n and x_{n-k} (k represents the delay index), i.e.,

$$y_n = \sum_{k=0}^{N} h_{1,k} x_{n-k} + \sum_{k=0}^{N} h_{2,k} x_{n-k}{}^2 + \sum_{k=0}^{N} h_{3,k} x_{n-k}{}^3, \quad (1)$$

where N corresponds to the maximum delay in the SI channel and $h_{i,k}$ ($i = 1, 2, 3$) is the i^{th} order digital canceller coefficient. Depending upon the SI channel, higher order nonlinear terms can be included ((1) only includes up to the 3^{rd}-order non-linearity). Using a pilot data sequence, the digital SI canceller coefficients can be found by solving the least-square problem. Using the described approach, we implemented the digital SIC algorithm in NI LabVIEW, and demonstrated it in [3].

4. ALGORITHMS AND RATE GAINS

Starting with realistic models of FD hardware described in previous sections, there are a few basic questions to ask: (i) How much SIC is needed for FD to improve the rates? (ii) If we have an FD radio with a given residual SI profile



(a) (b)

Figure 4: (a) Definition of rate improvement and (b) maximum rate improvement for equal SNRs on UL and DL.

(see, e.g., Fig. 2(c)), in what cases do we benefit from using it? (iii) How much rate improvement can we expect from a given FD radio, and under what circumstances?

To address these questions, we considered multiple orthogonal frequency channels (as in, e.g., OFDM) and modeled the residual SI as a constant fraction of the TX power level on the corresponding channel, which is consistent with the implementations described in Sections 2 and 3. We considered the problems of (i) maximizing the sum of uplink (UL) and downlink (DL) rates of an FD link [7] and (ii) determining the capacity region of an FD link[1] [8]. We obtained a number of insightful analytical results and also developed power allocation algorithms for these problems.

Since the promise of FD is to potentially double the sum of UL and DL rates, the problem of sum rate maximization from [7] provides us with the understanding of when it makes sense to use FD and how much can be gained in the best case. The problem of finding the capacity region of an FD link from [8] allows us to understand UL and DL rate allocation and possible gains under Quality of Service (QoS) requirements. Additionally, the properties of the capacity region and algorithms for determining it are essential building blocks for future FD-enabled MAC layer protocols.

To measure the rate improvement of an FD rate pair (r_b, r_m), we defined it as the number p for which $\left(\frac{r_b}{p}, \frac{r_m}{p}\right)$ is at the boundary of the corresponding time-division duplex (TDD) capacity region [7, 8].

4.1 Sum Rate Maximization

We first considered the problem of allocating TX power levels to the mobile station (MS) and the base station (BS) communicating over an FD link to maximize the sum of the UL and DL rates on a *single channel*. In this case, the sum rate r is neither convex nor concave in the TX power levels. However, we proved that *if there exists an FD rate pair (r_b, r_m) whose sum is higher than the maximum TDD rate, then $r_b + r_m$ is maximized when both TX power levels are set to their respective maximum values.*

We also obtained a condition for the sum rate r as a function of TX power levels under which r has structure that allows its maximization to be addressed in the general multi-channel setting. We showed that when this condition does not hold, FD cannot provide high rate improvements. The condition states that *the SI should be cancelled by at least the same amount as the wireless channel attenuates the TX signal on the path to the intended RX.* Fig. 4(b) shows attainable rate improvements when UL and DL signal-to-noise ratios (SNRs) are equal and self-interference-to-noise-ratio (XINR) at the BS is equal to 0 dB. As Fig. 4(b) suggests, similar to the stated condition, UL and DL SNRs need to be at least as high as the XINR at the MS.

In general, the problem of power allocation over multiple orthogonal channels to maximize the sum rate is non-convex and difficult for the existing optimization techniques. However, using structural properties of the sum rate that we proved, we developed an algorithm that under mild restrictions in practice converges to a global optimum. We also evaluated the developed algorithm against simple power allocation policies on measured residual SI values for the conventional canceller described in Section 3.1.1.

Interestingly, our results suggest that *when FD provides appreciable gains, simple power allocation policies suffice.*

4.2 Capacity Regions of FD Links

The power allocation that maximizes the sum rate only provides a single rate pair. In practice, however, the rate requirements on UL and DL may differ significantly from the rate pair provided by the sum rate maximization. Thus, it is important to understand what FD rate pairs are attainable, i.e., to understand the capacity region of an FD link.

One way of obtaining different combinations of UL and DL rates is through different power allocations. The FD capacity regions we can obtain in such a manner will in general be non-convex. However, legacy TDD systems have the capability of time sharing. Therefore, it is possible to obtain the convex hull of an FD capacity region through time sharing between different FD rate pairs. We refer to such a region as the time-division FD (TDFD) capacity region. Notice that a TDFD capacity region in general provides higher rates than the corresponding FD region. Moreover, having a convex capacity region is desirable for the design of MAC protocols, as most scheduling algorithms rely on this assumption.

In [8], we obtained several analytical and algorithmic results that characterize FD and TDFD capacity regions in both single-channel and multi-channel scenarios. For general power allocation over multiple channels, the problem of determining (either FD or TDFD) capacity region is non-convex. However, we obtained an algorithm (AltMax) that in practice determines the TDFD region under mild restrictions. We also developed a low-complexity heuristic.

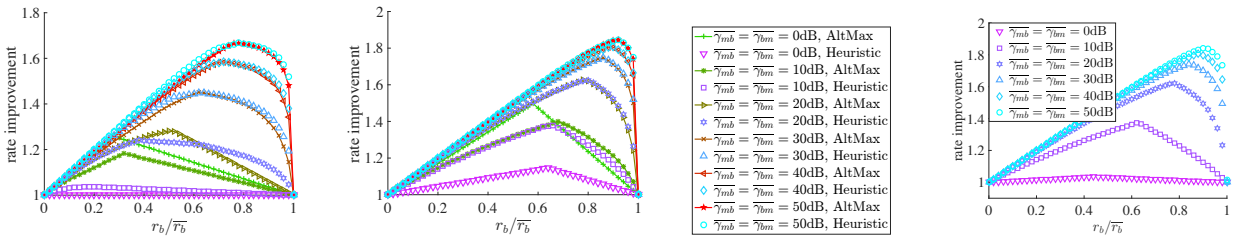
Figs. 5(a) and 5(b) show the rate improvements over TDFD capacity regions computed by AltMax and the heuristic, for the BS FD receiver from [2], the MS FD receivers whose SIC is shown in Fig. 2(a), and different values of average UL and DL SNRs $\overline{\gamma}_{mb}$ and $\overline{\gamma}_{bm}$. For comparison, we also show the rate improvements when the power levels are allocated equally over the channels at both stations, for FDE-based MS FD receiver described in Section 3.1.2 (Fig. 5(c)). As Fig. 5 suggests, *whenever the rate improvements are high, equal power allocation over channels is near-optimal. For low to medium rate improvements, a simple power and time allocation heuristic suffices.*

5. OUTSTANDING CHALLENGES

Our work has addressed many of the fundamental challenges associated with the development of practical FD wireless systems. However, many open challenges remain, and we review some of them in this section.

Integrated FD transceivers. While the initial results are promising, there is a need to further improve the performance of integrated SI-cancelling FD transceivers. In

[1]The capacity region of an FD link is defined as the set of all attainable UL and DL rate pairs.



(a) (b) (c)

Figure 5: Rate improvements for BS FD receiver from [2] and (a) conventional MS FD receiver (see Section 3.1.1), (b) FDE-based MS FD receiver (see Section 3.1.2), (c) FDE-based MS FD receiver and equal power allocation over channels.

particular, scaling of cancellation bandwidth up to and beyond 80 MHz for emerging wireless standards and handling of more powerful SI at the receiver input (>+10 dBm) represent important open problems.

Fairness in CSMA-type protocols. CSMA lays the foundation for the distributed 802.11 protocols. Therefore, it is important to understand the performance of these protocols when the network is shared between the legacy HD users and new FD users. In particular, it is of utmost importance to understand the following questions: *How should the back-off times be chosen for HD and FD users? (Should they be the same?) What is the right notion of fairness among the HD and FD users? What is the trade-off between the fairness and rate improvements?*

Network-wide resource allocation and scheduling in OFDMA systems. Current cellular systems are OFDMA, where orthogonal frequency channels are shared among multiple users at a time. Choosing how to allocate the channels to users over time is a challenging problem that has not been addressed yet. However, for FD to become a part of future cellular and small cell standards, *it is essential to address the challenges associated with the network-wide channel, power, and time allocation, taking into account QoS considerations for different classes of traffic.*

Experimental evaluation. As discussed in Section 3.1, the problem of adaptive analog SIC is more challenging for wideband (FDE-based) cancellers than for the narrowband (conventional) canceller. Hence, to support FD in wideband standards such as Wi-Fi and LTE, *it is necessary to develop adaptive SIC algorithms for FDE-based cancellers that can run in real time.* Finally, *there is a need for experimental evaluation of scheduling, power control, and channel allocation algorithms tailored to the special characteristics of full-duplex wireless networks and systems.*

6. CONCLUSION

We discussed the challenges imposed by the design of IC-based FD systems and presented some of the results obtained in the FlexICoN project [1]. We also outlined some of the open problems in the area. The recent results demonstrate that the challenges associated with FD, although steep, are not insurmountable. Hence, we believe that they will be addressed, thereby leading to higher rates and more flexible spectrum use in the emerging 5G networks.

7. ACKNOWLEDGMENTS

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