Demo Abstract: Full-Duplex with a Compact Frequency Domain Equalization-based RF Canceller

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***Abstract*—This demonstration presents a practical real-time full-duplex wireless link consisting of two full-duplex transceivers. Our prototyped full-duplex transceiver contains a custom-designed RF self-interference canceller and a National Instruments (NI) Universal Software Radio Peripheral (USRP). The discrete-component-based RF self-interference canceller emulates a compact RFIC implementation, which uses programmable bandpass filters to achieve wideband cancellation through the technique of frequency domain equalization. We demonstrate self-interference suppression across the antenna, RF, and the digital domains through the NI LabVIEW interface.**

***Index Terms*—Full-duplex wireless, frequency domain equalization, self-interference cancellation, software defined radio.**

I. Introduction

Full-duplex (FD) communication is an emerging wireless technology that holds a great promise of improving the wireless throughput. The concept of full-duplex communication is simple: a single device can simultaneously transmit and receive on the same frequency channel. However, as the transmitted signal is many orders of magnitude stronger than the desired signal at the input of the receiver, it is extremely challenging to recover the desired signal and enable such a communication. In particular, the self-interfering (SI) signal needs to be suppressed by a factor of a billion to a trillion, requiring $90 - 120\,\mathrm{dB}$ of self-interference cancellation (SIC).

Recent work has demonstrated SIC and the implementation of FD transceivers using off-the-shelf components (e.g., [1]–[3]). Our work focuses on Integrated Circuit (IC) implementations that are more appropriate for mobile and small-form-factor devices [4]–[6]. To assess the benefits of using FD, related work investigated achievable rate gains assuming perfect SIC [7] and non-negligible SI [8], where the latter uses realistic models of FD circuits.

In [9], we presented an implementation of an FD transceiver using a frequency-flat amplitude and phase-based RF SI canceller, which can only emulate the antenna interface isolation at a single frequency point, resulting in a narrowband SIC. In this demonstration, we present a cross-layered implementation of an FD wireless link composed of two FD transceivers that use *wideband frequency domain equalization-based (FDE-based) RF SI cancellers* [4].

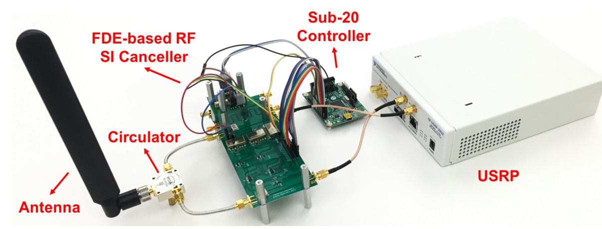
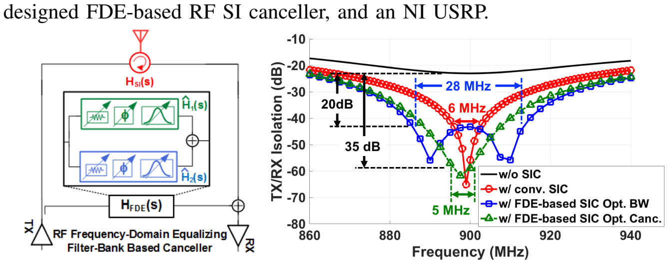


Fig. 1: An FD transceiver composed of an antenna, a circulator, a custom-designed FDE-based RF SI canceller, and an NI USRP.



(a) (b)

Fig. 2: (a) Block diagram of the presented FDE-based RF SI canceller. (b) Measured TX/RX isolation magnitude responses using the frequency-flat and the FDE-based RF SI cancellers implemented using discrete components.

Fig. 1 shows the implementation of an FD transceiver consisting of an antenna, a circulator, a National Instruments (NI) USRP, and an FDE-based RF SI canceller. Our compact FDE-based RF SI canceller is implemented using discrete components and it emulates the behavior of a wideband IC RF canceller that we presented in [4]. The FD wireless link operates at carrier frequency of $900\,\mathrm{MHz}$. A host PC controls the USRP from NI LabVIEW, which both performs digital signal processing and provides a graphical user interface. By applying both RF SIC and a digital SIC algorithm, as well as through the isolation at the antenna interface, we demonstrate $95\,\mathrm{dB}$ overall SI suppression in practice, enabling an FD link budget of $+5\,\mathrm{dBm}$ average transmission power level.

II. SI Cancellation

The SIC is performed across the antenna, RF, and the digital domains. At the RF antenna interface, we use a circulator which allows a single antenna to be shared between the TX and the RX. The wideband RF SI canceller presented in [4] is based on FDE of the wireless SI channel (i.e., the circulator TX-to-RX leakage path). It taps a reference signal at the output of the power amplifier (PA) and performs SIC at the input of the low-noise amplifier (LNA) at the RX side. Fig. 2(a) shows the block diagram of the presented FDE-based canceller, in which multiple reconfigurable RF bandpass filters (BPFs) are included to channelize the desired signal bandwidth. *Within each channel, the reconfigurable BPF, along with a variable attenuator and phase shifter, mimics the magnitude, phase, the slope of the magnitude, and the slope of the phase (i.e., group delay) of the wireless SI channel.*

The FDE-based RF SI canceller (see Fig. 1) is implemented using discrete components and its parameters are digitally programmable by a SUB-20 controller through the USB interface. Each RF BPF uses a surface-mount coil inductor and a surface-mount thin film capacitor that resonate at around $900\,\mathrm{MHz}$ with impedance transformation networks at BPF input and output ports for a high quality factor. The center frequency and the quality factor of the RF BPF are made programmable by inserting varactors in the LC resonator and in the impedance transformation networks, respectively. Furthermore, an adaptive parameter configuration mechanism is implemented on the PC to automatically tune the parameters of the canceller so that it adjusts to environmental changes.

Fig. 2(b) depicts the measured resultant SIC of the implemented FDE-based canceller. The measurements are performed inside an anechoic chamber to provide a stable environment so that the FDE-based canceller can achieve its best performance. The canceller can be configured to achieve wideband RF SIC (curve labeled “Opt. BW”), or to achieve higher RF SIC in a smaller bandwidth (curve labeled “Opt. Canc.”). Fig. 2(b) shows that the FDE-based canceller achieves more powerful RF SIC when compared to the conventional frequency-flat canceller presented in [9]: it provides a $20\,\mathrm{dB}$ SIC bandwidth of $28\,\mathrm{MHz}$ (with “Opt. BW”), which is 4.67x improvement over the frequency-flat canceller, or a $35\,\mathrm{dB}$ SIC bandwidth of $5\,\mathrm{MHz}$ (with “Opt. Canc.”).

After the RF SIC, digital SIC further cancels the linear SI as well as the non-linear distortion products generated by the RX and the RF SI canceller. The digital SIC is based on a non-linear tapped delay line, and given the transmitted and received pilot sequence, the non-linear coefficient sequence is found by solving a least-square problem. The digital SIC is implemented in NI LabVIEW, and it achieves about $45\,\mathrm{dB}$ SIC in the digital domain. Ideally, we achieve at least $100\,\mathrm{dB}$ overall SIC, but the performance slightly degrades in real-world wireless environment, as we will show in Section III.

III. Demonstration

The demonstration setup contains two FD transceivers that transmit and receive simultaneously on the same frequency channel. Through the front panel of NI LabVIEW, demo participants can observe the visualized transmitted and received signal of each FD transceiver in both time and frequency domains. The transmitted signal has a bandwidth of $5\,\mathrm{MHz}$[1] with an average output power of $+5\,\mathrm{dBm}$. The received signal is shown after RF and digital SIC, respectively. Without SIC, the SI signal is too strong for the desired signal to be detected. Once the SI signal is suppressed close to the $-90\,\mathrm{dBm}$ noise floor, the desired signal is revealed.

[1]The NI USRP-2932 cannot support a higher bandwidth while the digital signal processing is running on the host PC. Therefore, we focus on achieving higher RF SIC using the FDE-based canceller within the $5\,\mathrm{MHz}$ bandwidth.

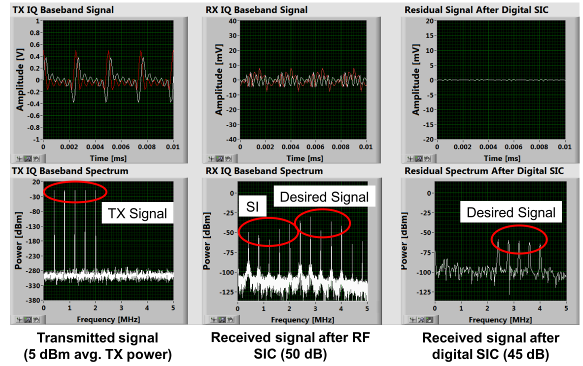


Fig. 3: The NI LabVIEW user interface showing the $+5\,\mathrm{dBm}$ transmitted signal (left), received signal at one FD transceiver with desired signal after RF SIC (middle), and recovered desired signal after digital SIC (right).

In this demonstration, a total amount of $95\,\mathrm{dB}$ SI suppression is achieved in practice, of which $50\,\mathrm{dB}$ is obtained by the circulator and the RF SI canceller across a $5\,\mathrm{MHz}$ bandwidth, and $45\,\mathrm{dB}$ is obtained by the digital SIC. Compared with the implementation in [9], this demonstration achieves (i) higher SIC in the RF domain by using a compact FDE-based RF SI canceller, and (ii) $5\,\mathrm{dB}$ higher overall SIC that supports $5\,\mathrm{dB}$ higher average transmission power level.

Acknowledgments

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