Full Duplex Circulator-Receiver Phased Array Employing Self-Interference Cancellation via Beamforming

Mahmood Baraani Dastjerdi, Negar Reiskarimian, Tingjun Chen,
Gil Zussman, and Harish Krishnaswamy
Department of Electrical Engineering, Columbia University, New York, NY, 10027, USA

***Abstract*— In this paper, we show how phased-array beamforming can be synergistically combined with full-duplex (FD) to achieve wideband RF self-interference (SI) suppression with minimal link budget (transmitter (TX) and receiver (RX) array gain) penalty and with no additional power consumption. An N-path-filter-based circulator-receiver FD front-end enables phased-array beamforming at baseband with minimal overhead by virtue of its multi-phase outputs. A 65nm CMOS scalable 4-element full-duplex circulator-receiver array is demonstrated that repurposes spatial beamforming degrees of freedom (DoFs) to achieve SI suppression, enabling (i) 50dB overall RF array self-interference cancellation (SIC) over 16.25MHz (WiFi-like) bandwidth (BW) with less than 3.5/3dB degradation in TX and RX array gains, respectively, across 8 elements, and (ii) 100dB overall array SIC suppression including digital SIC at +16.5dBm TX array power handling.**

I. Introduction & FD Ph.-Array Challenges

Full-duplex wireless has drawn significant research interest [1], but silicon-based implementations are plagued by low TX power handling, particularly in solutions that integrate the antenna interface [2]–[5]. Meanwhile, multiple-antenna phased-array technology is also drawing attention for 5G systems due to its ability to increase link range and reject spatial interference through beamforming. Combining the benefits of FD with multi-antenna technology is an important research challenge.

Phased arrays can substantially enhance range in FD links that are challenged from a TX power handling and RX noise perspective. An 8-element 730MHz array with +1dBm TX power per element (P_{TX}), 6dBi antenna gains, 15dB TX and RX array gains (AG_{TX} and AG_{RX}, 3dB degraded from ideal 18dB), 16.25MHz BW, 5dB RX noise figure (NF), 20dB required signal-to-noise ratio (SNR) and 10dB implementation losses can establish an FD link over 3.7km. However, combining FD operation with phased-array beamforming is a significant challenge because, aside from the SI from each TX to its own RX, there exists *cross-talk self-interference (CTSI)* between every TX-RX pair (Fig. 1).

In the worst case, the SI and CTSI can add up constructively in each RX channel and increase in power by N^2 (the TX array gain), and then add up constructively across RX channels to increase in power by another N^2 (the RX array gain), resulting in a total of N^4 increase in SI levels relative to a single-element transceiver. *Therefore, while phased-array beamforming provides N^2 increase in array gain at both the TX and RX, it could also potentially increase the SI levels by a similar amount*, although the actual combined SI level is dependent on the $N \times N$ SI channel matrix. The required array SIC can be calculated as $SIC_{\mathrm{array}} = P_{\mathrm{TX}} \cdot AG_{\mathrm{TX}} \cdot AG_{\mathrm{RX}}/N_{\mathrm{floor}} = 119$dB, where $N_{\mathrm{floor}} = kT \cdot BW \cdot NF \cdot N = -88$dBm is the receiver array noise floor referred to the antenna inputs.

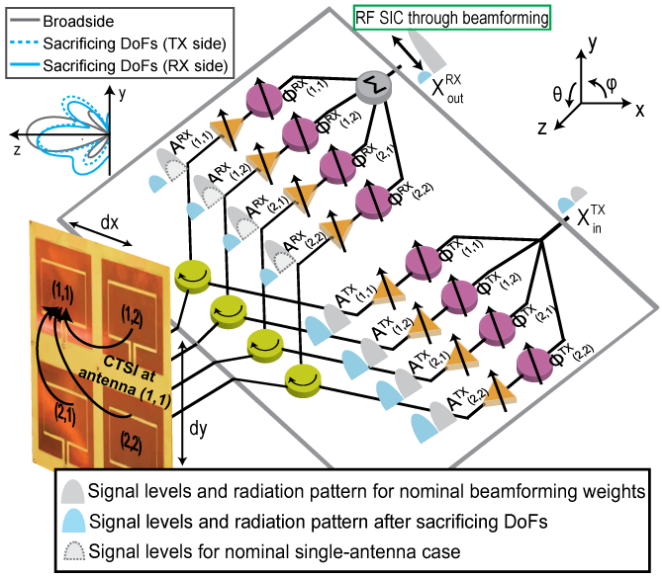

Fig. 1. Full-duplex phased-array transceiver achieving SIC through beamforming by sacrificing a few spatial DoFs.

II. Achieving SIC by Using Beamforming DoFs

Along with this challenge arises a unique opportunity – a phased-array transceiver with N antenna elements in general features $2(N-1)$ complex DoFs, $(N-1)$ each at the TX and RX, representing the complex-valued (amplitude and phase) weights applied at each element relative to the first element. These DoFs are typically used to set the TX/RX beam-pointing directions, as well as the directions of the nulls. However, one can sacrifice a few beamforming DoFs at the TX and RX so that *after TX and RX beamforming, the total SI is suppressed at the expense of some TX and RX beam characteristics*, such as a few nulls and/or some gain loss in the beam-pointing direction(s).

Combining FD with multi-antenna systems has been considered at the system-level in [6], [7]. However, (i) *jointly* optimizing TX and RX beamforming weights to achieve FD operation with *wideband SIC* has not been explored. Furthermore, (ii) this work considers *a shared TX-RX antenna array for the first time through the implementation of*

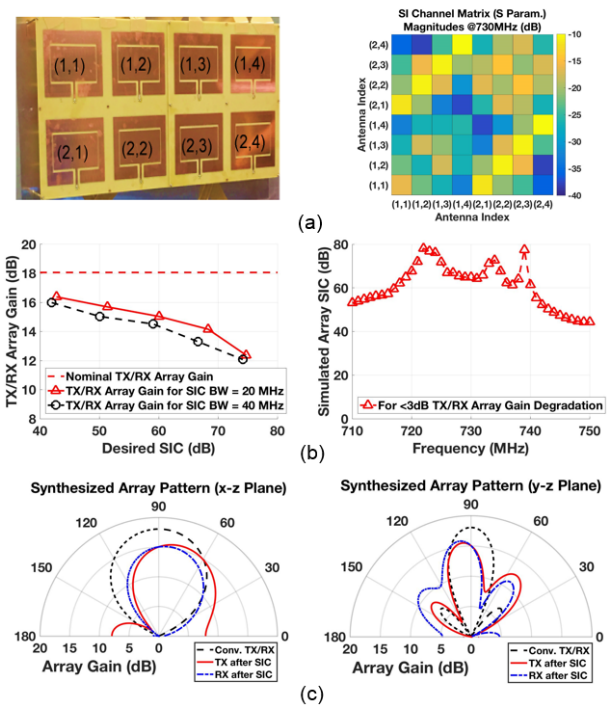

Fig. 2. (a) A 2×4 730MHz antenna array, (b) simulated TX/RX array gain for a desired array SIC based on an optimization algorithm using measured S-parameters, and (c) resultant TX/RX array patterns for 60dB array SIC across 20MHz.

integrated circulators. Moreover, (iii) this work considers SIC through *analog* beamforming for the first time, as well as (iv) *a scalable 65nm CMOS FD phased-array receiver*, where baseband beamforming is eased through the multi-phase outputs available in an N-path-filter-based circulator-receiver front-end [4].

Fig. 2(a) depicts a 2×4 rectangular array of slot loop antennas with $\lambda/2$ spacing at 730MHz as well as a depiction of the measured S-parameters at the center frequency. No special means were taken to increase the isolation between the antennas and the worst-case coupling is as low as -10dB. The measured S-parameters are used to construct the SI channel matrix, $\mathbf{H}^{\mathrm{SI}}$. The residual array SI after RX beamforming, $X_{\mathrm{out}}^{\mathrm{RX}}$, is given by (see Fig. 1)

$$X_{\mathrm{out}}^{\mathrm{RX}} = X_{\mathrm{in}}^{\mathrm{TX}} \cdot (\mathbf{w}^{\mathrm{TX}})^{\top} \cdot (\mathbf{H}^{\mathrm{SI}})^{\top} \cdot \mathbf{w}^{\mathrm{RX}}, \tag{1}$$

where $\mathbf{w}^{\mathrm{TX/RX}}$ are the TX/RX beamforming weight vectors. The far-field beamforming pattern can be calculated as

$$E^{\mathrm{TX/RX}}(\varphi,\theta) = \sum_{m=1}^{M}\sum_{n=1}^{N} w_{(m,n)}^{\mathrm{TX/RX}} \cdot e^{j\frac{2\pi}{\lambda}[(m-1)d_x \cos\theta\cos\varphi + (n-1)d_y \cos\theta \sin\varphi]}, \tag{2}$$

where d_x and d_y are the distances between the antennas in the horizontal and vertical directions. The objective is to find the normalized (complex-valued) TX and RX beamforming weight vectors, $\mathbf{w}^{\mathrm{TX}}$ and $\mathbf{w}^{\mathrm{RX}}$, that both (i) *maximize the TX and RX array gains in the far-field* (2), and (ii) *achieve wideband SIC in the near-field* (1). An optimization problem is formulated and solved to minimize TX and RX array gain degradation (essentially sacrificing nulls) while ensuring a desired $SIC_{\mathrm{array}} = P_{\mathrm{TX}} + AG_{\mathrm{TX}} - (P_{\mathrm{SI}} - AG_{\mathrm{RX}})$ after TX and RX beamforming, where P_{SI} is the residual SI. Fig. 2(b) depicts the results of the optimization for broadside beam-pointing, indicating a clear but favorable trade-off between beamforming gain and SIC. It is possible to achieve $>$ 60dB array SIC over 20MHz BW for $<$ 3dB TX/RX array gain degradation. The resultant array patterns are shown in Fig. 2(c). It can also be seen in Fig. 2(b) that ensuring SIC across wider BWs results in slightly higher TX/RX array gain degradation.

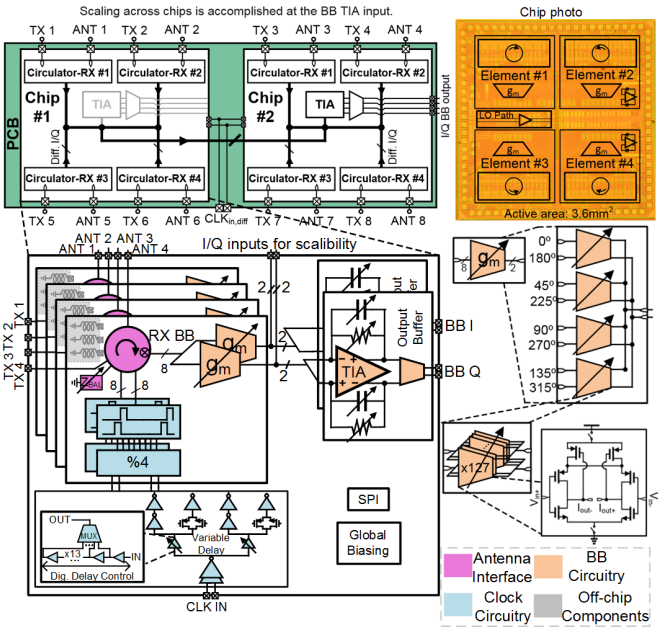

Fig. 3. Block/circuit diagram and chip photo of the 65nm CMOS 730MHz 8-element FD circulator-receiver phased-array system employing scalable 4-element ICs.

Four important features must be highlighted: (i) SI suppression is essentially achieved in the *spatial domain* through a trade-off between near-field SI nulling and far-field beamforming without any explicit cancellers and associated power consumption, since the TX/RX beamformers are repurposed, (ii) the SI suppression is *wideband* since different antenna coupling paths are cancelling each other, as opposed to having an IC canceller duplicating the frequency characteristics of an antenna coupling path, (iii) the beamforming-FD trade-off can be *dynamically adapted in the field*, with the number of DoFs sacrificed depending on the required SI cancellation, bandwidth, external interferers that need to be nulled etc., and (iv) the trade-off between FD and beamforming will become more favorable for larger antenna arrays.

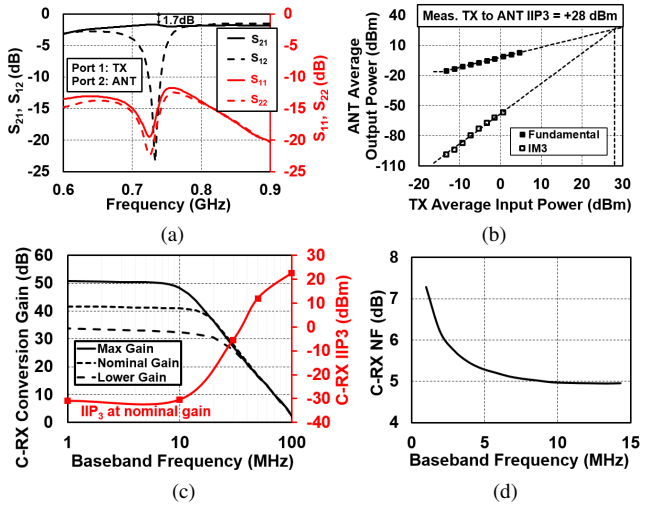

Fig. 4. Single-element C-RX measurements: (a) TX-ANT S-parameters demonstrating nonreciprocity, (b) TX-ANT IIP3, (c) ANT-baseband conversion gain, IIP3 and (d) NF versus baseband frequency.

III. Implementation and Measurement Results

A scalable 65nm CMOS 730MHz 4-element circulator-RX (C-RX) phased array is implemented (Fig. 3). The array uses the N-path-filter-based combined-circulator-RX concept described in [4]. *The availability of* 8*-phase baseband nodes in each C-RX further simplifies the RX beamforming*, as 7-bit programmable g_m cells are implemented for each baseband (BB) node in each C-RX and then combined in the current domain across all 4 elements into low-input impedance IQ TIAs (implemented using two-stage op-amps) to enable Cartesian beamforming. The low input impedance combining point is also brought to pads to facilitate scaling across chips. To tile two chips, the TIAs in the second chip would be turned off, and the current from its g_m cells would be combined into the TIAs of the first chip, with the low impedance providing resiliency to board trace capacitance. The g_m cells use the inverter-based design introduced in [8] where saturation-region PMOSes provide both common-mode rejection and feedback. This is particularly useful here as the g_m cell outputs are connected to PCB traces for scaling, making more elaborate common-mode feedback circuits hard to stabilize.

The C-RXs exhibit 1.7dB TX-ANT loss, +28dBm TX-ANT IIP3, 41dB nominal single-element ANT-BB conversion gain, −31dBm/+22.5dBm in-band/out-of-band ANT-BB IIP3 and 5dB single-element NF (Fig. 4). Array FD measurements are performed with the 2×4 rectangular array of slot loop antennas described earlier (Fig. 5). Two ICs are tiled on PCB to realize an 8-element FD C-RX phased array, and a custom 8-element phased-array TX PCB is built using discrete components. The isolation of each C-RX is around 15dB. When the TX and RX arrays are configured for nominal broadside beamforming, the average array SIC over 16.25MHz is 23dB. When the TX and

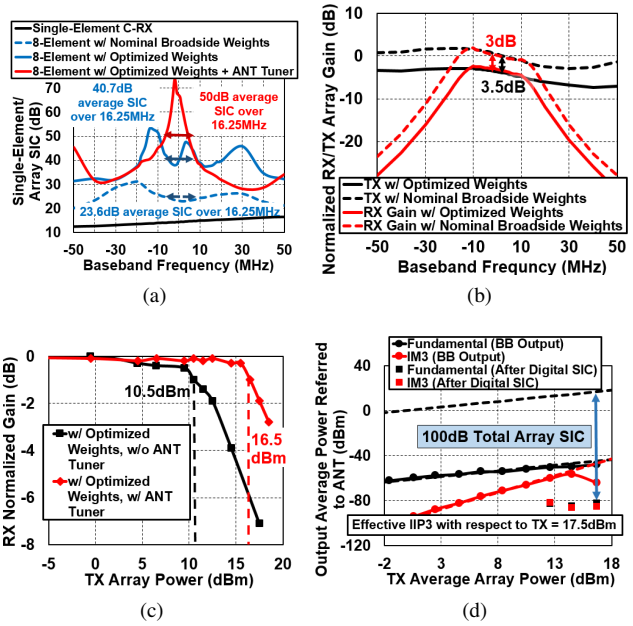

Fig. 5. Measured full-duplex phased-array performance across 8-elements (tiling of 2 ICs): (a) array SIC, (b) impact of optimized weights to achieve SIC on the TX/RX array gain, (c) gain compression of a small received signal under the influence of TX power with optimized weights with and without the antenna tuner, and (d) two-tone TX test tracking the TX total SI and its IM3 products at the receiver output with additional digital SIC.

RX arrays are configured to sacrifice beamforming DoFs for SIC based on the optimization code described earlier while allowing 3dB TX and RX array gain loss, 40.7dB array SIC is achieved over 16.25MHz. The profile is very wideband, and very similar to the simulated profile shown in Fig. 2, albeit at somewhat lower SIC levels, due to the fact that those simulations neglected the circulator's internal isolation, quantization of beamforming weights, etc. Finally, custom-designed tuners are integrated with the antennas and co-optimizing the tuners (configured identically across all elements) yields 50dB array SIC over 16.25MHz. The RX and TX array gains are measured across frequency for broadside excitation with these beamforming weights optimized for SIC, and the 3dB array gain loss is verified. The synthesized TX and RX array patterns for these weights are depicted in Fig. 2.

With the beamforming and SIC thus configured, and the TX array power ($P_{\mathrm{TX}} \cdot AG_{\mathrm{TX}}$) swept, the gain imparted to a weak in-band signal radiated towards the array is monitored. 1dB compression of the weak in-band signal occurs at +16.5dBm, which can be inferred as the TX array power handling. Finally, two-tone TX tests are performed with beamforming and SIC configured, and the RX BB outputs are monitored. The effective IIP3 referred to the TX array power is +17.5dBm, and at +16.7dBm average TX array power, nonlinear Volterra-series-based digital SIC is able to suppress the residual total SI and its associated IM3 to below −84dBm, indicating 100dB total array SIC. Another 19dB of SIC is required to suppress the SI to the array noise floor

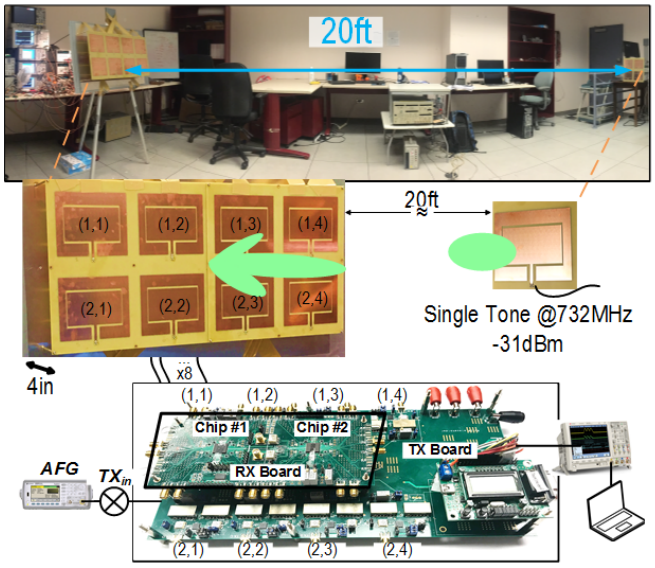

Fig. 6. Wireless FD demonstration setup.

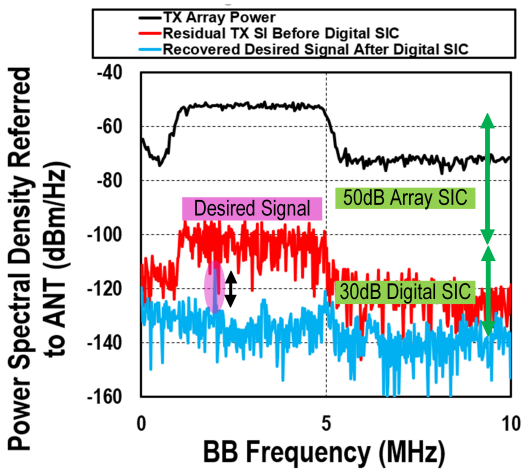

Fig. 7. Demo results: A -31dBm desired 732MHz continuous wave signal radiated from 20ft away from a single antenna is recovered while transmitting a 5MHz OFDM-like signal with $+8.7$dBm TX array power.

(on the effective IIP3 graph, the noise floor would be at $N_{\text{floor}}/AG_{\text{RX}} = -103$dBm), and can be potentially achieved with additional analog SIC.

Figs. 6 and 7 show a demo where a -31dBm desired 732MHz continuous wave signal radiated from 20ft from a single antenna is recovered while transmitting a 5MHz OFDM-like signal at $+8.7$dBm TX array power.

Table. I compares this work to the state of the art. Thanks to the combination of FD with phased-array beamforming, this work features higher RF and total SI suppression, higher TX array power handling, and superior potential FD link range.

IV. Conclusion

This work demonstrated how phased-array beamforming can be combined with FD operation to achieve wideband RF SIC with minimal link budget penalty and with no additional power consumption. The concepts were demonstrated through measurements using a 65nm CMOS scalable 4-element full-duplex circulator-receiver array. Topics for future research include exploring these concepts in massive antenna arrays, exploring co-design opportunities with the antenna array, and extending to full-duplex MIMO systems.

TABLE I
Comparison with state-of-the-art FD receivers with an integrated shared antenna interface.

		JSSC 2015 [2]	JSSC 2017 [3]	ISSCC 2017 [4]	This Work
	Architecture	Mixer-first TRX with Active Baseband Duplexing	RX with integrated magnetic-free N-path-filter-based circulator and BB SIC	Magnetic-free N-path-filter-based circulator-receiver with on-chip balance network	Full-duplex phased-array with integrated magnetic-free N-path-filter-based circulator-receivers
RX metrics	RX Frequency Range	0.1-1.5GHz	0.6-0.8GHz	0.61-0.975GHz	0.61-0.975GHz
	Number of Antenna Paths	1	1	1	4 per IC, 2 ICs tiled for FD measurements
	Gain	53dB	42dB	Max: 43dB Nominal: 28dB	Max: 51dB Nominal: 41dB (single-element)
	Noise Figure	5-8dB	8.4dB	6.3dB	5dB (single-element)
	OOB IIP3	+22.5dBm	+19dBm	+15.4dBm	+22.5dBm (single-element, 100MHz offset)
FD Metrics	Integrated SI Suppression Domains	Analog BB	RF + Analog BB	RF	RF + Spatial
	Amount of Integrated SI Suppression	33dB across 300kHz TX BB BW	42dB SIC across 12MHz BW	40dB SIC across 20MHz BW	50dB array SIC across 16.25MHz BW (Across 8 elements)
	Effective IIP3 with respect to TX Power	~0dBm at 43/53dB gain[1]	+1dBm at 42dB gain	+9dBm at 26dB gain	+17.5dBm (TX Array Power)
	Overall TX Port Power Handling	-17.3dBm[2]	-7dBm	+7dBm[2]	+16.5dBm[2] (TX Array Power)
	RX Degradation in Full-Duplex Mode	~2-5dB[3]	2.5dB	1.7dB	3dB (Array Gain Degradation)
	Overall SI Suppression	33dB	85dB (incl. digital SIC)	80dB (incl. digital SIC)	100dB array SIC (incl. digital SIC)
Resources	RX Power	43-56mW (incl. TX)	100mW signal path (10mW LO + 30mW BB canceller)	72mW	32mW for 4 elements on an IC
	Antenna Interface Power	Incl. in RX power	59mW (at 0.7GHz)	36mW (at 0.7GHz)	26.25mW per element
	Technology	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS
	Active Area	1.5mm^2	1.4mm^2	0.94mm^2	3.6mm^2 (0.9mm^2 / element)

1. From Fig. 31(a) in the paper. 2. Limited by ~1dB gain compression induced in the receive signal.
3. at -17.3dBm TX power.
N/A: Not Applicable N/R: Not Reported

Acknowledgment

This work was sponsored by Intel and the NSF EARS program. The authors would like to thank Dr. Stefano Pellerano for useful comments.

References

[1] J. Zhou *et al.*, "Integrated full duplex radios," *IEEE Communications Magazine*, vol. 55, no. 4, pp. 142–151, 2017.
[2] D. Yang *et al.*, "A wideband highly integrated and widely tunable transceiver for in-band full-duplex communication," *IEEE JSSC*, vol. 50, no. 5, pp. 1189–1202, May 2015.
[3] N. Reiskarimian *et al.*, "A CMOS passive LPTV nonmagnetic circulator and its application in a full-duplex receiver," *IEEE JSSC*, vol. 52, no. 5, pp. 1358–1372, 2017.
[4] N. Reiskarimian *et al.*, "Highly-linear integrated magnetic-free circulator-receiver for full-duplex wireless," in *IEEE ISSCC*, Feb 2017, pp. 316–317.
[5] S. Ramakrishnan *et al.*, "An FD/FDD transceiver with RX band thermal, quantization, and phase noise rejection and >64dB TX signal cancellation," in *IEEE RFIC*, 2017, pp. 352–355.
[6] E. Everett *et al.*, "Softnull: Many-antenna full-duplex wireless via digital beamforming," *IEEE Trans. Wireless Commun.*, vol. 15, no. 12, pp. 8077–8092, Dec 2016.
[7] J. P. Doane *et al.*, "Simultaneous transmit and receive with digital phased arrays," in *IEEE PAST*, Oct 2016, pp. 1–6.
[8] Y. Lien *et al.*, "A high-linearity CMOS receiver achieving +44dBm IIP3 and +13dBm B1dB for SAW-less LTE radio," in *IEEE ISSCC*, Feb 2017, pp. 412–413.