Self-Interference Cancellation via Beamforming in an Integrated Full Duplex Circulator-Receiver Phased Array

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***Abstract*—This paper describes how phased array beamforming can be exploited to achieve wideband self-interference cancellation (SIC). This SIC is gained with no additional power consumption while minimizing link budget (transmitter (TX) and receiver (RX) array gain) penalty by repurposing spatial degrees of freedom. Unlike prior works that rely only on digital transmit beamforming, this work takes advantage of analog/RF beamforming capability that can be easily embedded within an integrated circulator-receiver array. This enables (i) obtaining SIC through beamforming on both TX and RX sides, thus increasing the number of degrees of freedom (DoF) that can be used to obtain SIC and form the desired beams, while (ii) sharing the antenna array between TX and RX. A 750MHz 65nm CMOS scalable 4-element full-duplex circulator-receiver array is demonstrated in conjunction with a TX phased array implemented using discrete components. A tiled 8-element system shows (i) 50dB overall RF array SIC over 16.25MHz (WiFi-like) bandwidth (BW) with $< 3.5/3$dB degradation in TX and RX array gains, respectively, and (ii) 100dB overall array SIC including digital SIC, supporting $+16.5$dBm TX array power handling.**

I. Introduction

Over the past decade, the rapid growth of silicon-based phased array technology has started to make an impact on commercial and military wireless applications. Over the next decade, phased array and Multiple-Input-Multiple-Output (MIMO) radios are expected to emerge as a key technology for next-generation wireless networks. Phased arrays can provide coherent beamforming gain [1] and MIMO can significantly increase throughput [2]. Both technologies are a part of the upcoming standards for next-generation Wireless Local Area Networks (WLANs) [3] and 5G [4]. Meanwhile, Full-Duplex (FD) wireless – simultaneous transmission and reception on the same frequency channel – has drawn significant research interest, and is an emerging technology that can theoretically double the channel capacity [5], integrating FD capability with phased array transceivers can provide higher data rate and higher spectrum efficiency, while substantially enhancing link range.

Due to space constraints in both Wi-Fi Access Points (APs) and small cell Base Stations (BSs), there is a need for Integrated Circuit (IC) design and implementation of such transceivers. Although silicon-based implementations are plagued by low TX power handling, particularly in solutions that integrate the antenna interface with low TX-ANT loss [6]–[9], phased arrays can substantially enhance range. Based on link budget calculations shown in Table. I, an 8-element 730MHz array with +1dBm TX power per element (P_{TX}), 6dBi antenna gain, 15dB TX and RX array gains (AG_{TX} and AG_{RX}, 3dB degraded from the ideal 18dB array gain), 16.25MHz bandwidth (BW), 5dB RX noise figure (NF), 20dB required Signal-to-Noise Ratio (SNR) and 10dB implementation losses can establish an FD link over a distance of 3.7km.

TABLE I: Link budget calculations.

Metric	Calculation	Value
Frequency (f)		730MHz
# of ANT Elements (N)		8
TX Power per Element (P_{TX})		1dBm
TX Array Gain (AT_{TX})	$N^2 - 3$dB	15dB
TX ANT Gain (G_{TX})		6dBi
Bandwidth (BW)		16.26MHz
RX Noise Figure (NF)		5dB
RX Array Gain (AG_{RX})	$N^2 - 3$dB	15dB
RX ANT Gain (G_{RX})		6dBi
RX Array Noise Floor referred to the ANT Input (N_{floor})	$kT \cdot BW \cdot NF \cdot N$	-88dBm
Required SNR		20dB
RX Array Sensitivity referred to the ANT Input (P_{sense})	$N_{\mathrm{floor}} \cdot SNR$	-68dBm
Implementation Losses (IL)		10dB
Supported Range ($R_{\max}$)	$\frac{\lambda}{4\pi}(P_{\mathrm{TX}} AG_{\mathrm{TX}} G_{\mathrm{TX}} \cdot AG_{\mathrm{RX}} G_{\mathrm{RX}} \cdot IL/P_{\mathrm{sense}})^{1/2}$	3.7km
Required Array SIC (SIC_{array})	$P_{\mathrm{TX}} AG_{\mathrm{TX}} AG_{\mathrm{RX}}/N_{\mathrm{floor}}$	119dB

Multi-antenna FD operation is extremely challenging as not only the SI from each TX to its own RX needs to be cancelled, but also the cross-talk SI (CTSI) needs to be suppressed between *every TX-RX pair* (Fig. 1). Indeed, the total SI power level at the RX side output of an N-element FD phased array with shared antenna interface can potentially be N^4 times higher relative to a single-element transceiver, since the SI and CTSI from every TX element can add up constructively at an RX element and increase in power by N^2 (the TX array gain), and then increase by another N^2 across the RX elements (the RX array gain). Hence, the required array SIC can be calculated as $SIC_{\mathrm{array}} = P_{\mathrm{TX}} AG_{\mathrm{TX}} AG_{\mathrm{RX}}/N_{\mathrm{floor}} = 119$dB, where $N_{\mathrm{floor}} = kT \cdot BW \cdot NF \cdot N = -88$dBm is the array receiver noise floor referred to the antenna input. *In other words, although phased array beamforming provides N^2 increase in array gain at both the TX and RX, it could also potentially increase the SI levels by a similar amount*. However, the actual combined SI level depends on the $N \times N$

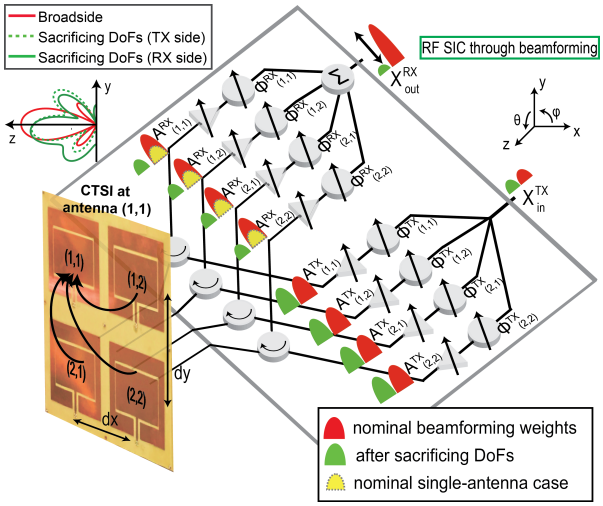
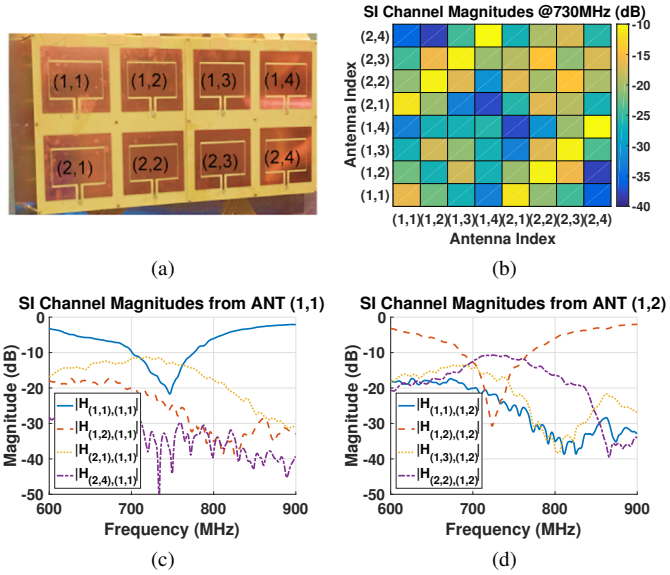


Fig. 1: Full-duplex phased array transceiver achieving SIC through TX and RX beamforming by sacrificing a few spatial DoF.



(a) (b) (c) (d)

Fig. 2: (a) A 2×4 8-element antenna array at 730MHz with $\lambda/2$ spacing, (b) the measured SI channel magnitudes at 730MHz, and (c), (d) examples of measured SI channel magnitudes across frequency from antenna elements $(1,1)$ and $(1,2)$ to the adjacent elements, respectively.

SI channel matrix as well as TX/RX beamforming weights. In this work, we manipulate beamforming weights to achieve wideband SIC while minimizing the penalty on the TX and RX array gains [10]. In [10], we mainly discussed the IC design of Circ.-RX array. In this invited paper, we discuss (i) link budget calculation, (ii) design and implementation details of the 8-element phased array TX made using discrete components, (iii) slot loop antenna design, and (iv) how Circ.-RX, TX and slot loop antenna are integrated to form FD phased array transceiver.

Combining FD with multi-antenna systems has been investigated at the system-level in [11], [12]. However, this work explores the joint optimization of TX and RX beamforming weights to achieve wideband SIC for FD operation. In addition, this work considers a shared TX-RX antenna interface through integrated circulators. Furthermore, the custom IC designed enables performing analog beamforming to achieve SIC for the first time. Specifically, a scalable 65nm CMOS FD circulator-receiver array is introduced [10], where beamforming is performed in the baseband (BB) in a high-linearity and low-noise manner with little overhead by employing the multi-phase outputs available in an N-path-filter-based circulator-receiver front-end [8].

II. SIC through Beamforming

An N-element phased array transceiver with a shared antenna interface and control over phase and amplitude of each element on both transmit and receive features overall $2(N-1)$ complex-valued DoF on TX and RX sides ($(N-1)$ DoF on each side). These DoF are a representation of the complex-valued weights (amplitudes and phases) of each element relative to that of the first element. Typically, these DoF are employed to form the beams toward desired node location, and minimize interference to/from nearby radios by pointing nulls towards them or suppressing the side-lobes of the radiation pattern. Alternatively, a few beamforming DoF at the TX and RX can be repurposed so that total SI is suppressed after RX beamforming at the expense of some TX and RX beam characteristics, such as a few nulls and/or some gain loss in the beam-pointing direction(s).

Fig. 2 depicts our implementation of a 2×4 rectangular array of slot loop antennas at 730MHz with $\lambda/2$ spacing, whose SI channel matrix is denoted by $\mathbf{H}^{\mathrm{SI}} = \left[H^{\mathrm{SI}}_{(m,n)}\right]$. As Fig. 2 shows, the antenna matching is around -20dB at the center frequency of 730MHz, while the magnitude of the SI channel from the closest element can be as high as -10dB (e.g., $|H_{(2,1),(1,1)}|$ from element $(1,1)$ to element $(2,1)$). Moreover, a vertical pair of elements have higher SI channel magnitude than a horizontal pair of elements (e.g., $|H_{(2,1),(1,1)}| > |H_{(1,2),(1,1)}|$ at 730MHz).

Let $x(t)$ be the transmit signal in the time domain, and $\mathbf{w}^{\mathrm{TX}} = \left[w^{\mathrm{TX}}_{(m,n)}\right]$ and $\mathbf{w}^{\mathrm{RX}} = \left[w^{\mathrm{RX}}_{(m,n)}\right]$ be the complex-valued TX and RX beamforming weight vectors, respectively. Then, the phased array SI after RX beamforming, $x^{\mathrm{SI}}(t)$, is given by

$$x^{\mathrm{SI}}(t) = (\mathbf{w}^{\mathrm{RX}})^{\top} \cdot \mathbf{H}^{\mathrm{SI}} \cdot \mathbf{w}^{\mathrm{TX}} \cdot x(t), \tag{1}$$

where $(\cdot)^{\top}$ denotes the transpose of a vector.

Consider a 3D coordinate system where the 2×4 rectangular array is located on the x-y plane. We denote the TX and RX beamforming directions by the azimuth and elevation angles (ϕ, θ) in a horizontal coordinate system. Then, the *far-field* array TX/RX beamforming pattern is given by

$$E^{\mathrm{TX/RX}}(\phi,\theta) = (\mathbf{s}^{\mathrm{TX/RX}}(\phi,\theta))^{\top} \cdot \mathbf{w}^{\mathrm{TX/RX}} \tag{2}$$
$$= \sum_{m=1}^{2}\sum_{n=1}^{4} w^{\mathrm{TX/RX}}_{(m,n)} \cdot e^{j\pi[(m-1)\cos\phi\cos\theta + (n-1)\sin\phi\cos\theta)]},$$

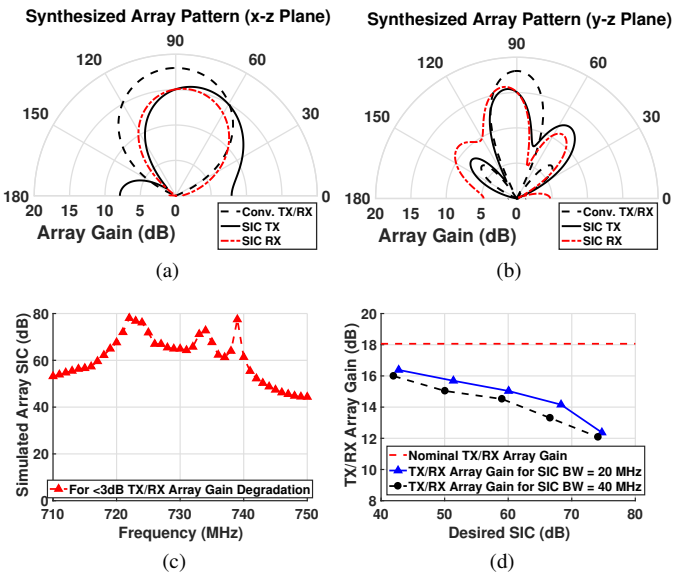


Fig. 3: (a), (b) Simulated TX/RX array patterns in the x-z and y-z planes while achieving 60dB array SIC across 20MHz with 3dB array gain degradation in the TX/RX broadside beam-pointing directions, (c) simulated array SIC where at least 60dB SIC is guaranteed to be achieved across 720-740MHz, and (d) simulated TX/RX array gain for a desired array SIC based on solving an optimization problem using the measured SI channels depicted in Fig. 2.

where

$$\mathbf{s}^{\mathrm{TX/RX}}(\phi,\theta) = \left[s^{\mathrm{TX/RX}}_{(m,n)}(\phi,\theta)\right] = \left[e^{j\pi[(m-1)\cos\phi\cos\theta+(n-1)\sin\phi\cos\theta]}\right],$$

denotes the TX/RX beam steering vector. The goal is to achieve wideband SIC in the *near-field* (1) with minimal penalty of the TX/RX beamforming gains in the *far-field* (2). We formulate and solve an optimization problem where the objective is to maximize the TX and RX array gains, subject to the constraint that a desired amount of array SIC is achieved after TX beamforming.

We evaluated this idea through simulations using the measured array SI channel (see Fig. 2) and the results are summarized in Fig. 3. In the simulation, the TX/RX array gains are maximized for broadside beamforming (i.e., $\theta = 90°$) subject to the constraint that at least 60dB array SIC is achieved between 720-740MHz. Figs. 3(a) and 3(b) show that an array gain degradation of only 3dB compared with the maximal array gain of $N^2 = 18$dB can be maintained while achieving 60dB array SIC across 20MHz. Moreover, Fig. 3(d) shows the tradeoff between the maximum achievable TX/RX array gain for different amounts of desired array SIC across 20MHz and 40MHz, respectively.

In general, four important features must be highlighted: (i) SI suppression is essentially achieved in the *spatial domain* through a trade-off between near-field SI nulling and far-field beamforming without any explicit cancellers and associated power consumption, since the RX/TX beamformers are repurposed, (ii) the SI suppression is *wideband* since different

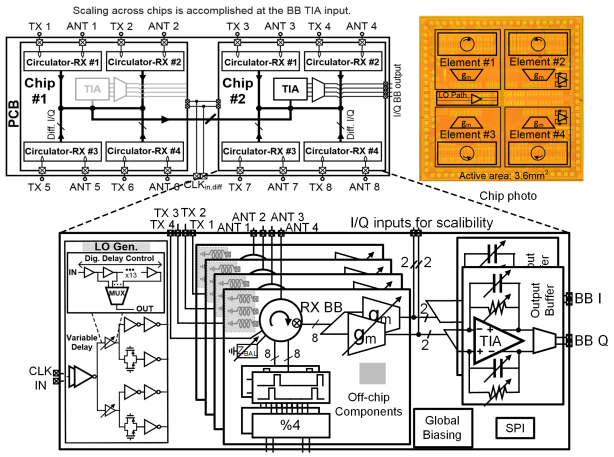


Fig. 4: Block/circuit diagram and chip photo of the 65nm CMOS 730MHz 8-element FD circulator-receiver (C-RX) phased array system employing scalable 4-element ICs.

antenna coupling paths are cancelling each other, as opposed to having an IC canceller duplicate the frequency characteristics of an antenna coupling path, (iii) the beamforming-FD trade-off can be *dynamically adapted* in the field, with the number of DoF sacrificed dependent on the required SI cancellation, bandwidth, external interferers that need to be nulled, etc., and (iv) the trade-off between FD and beamforming will become more favorable for larger arrays.

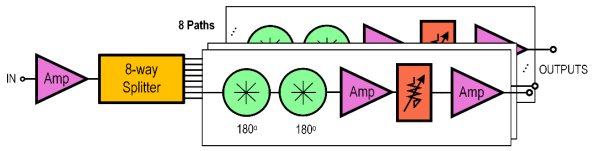
III. Implementation

A. Integrated Circulator-Receiver Phased Array

The N-path-filter-based combined-circulator-RX concept described in [8] provides the unique feature of having 8-phase baseband nodes available in each circulator-RX (C-RX) which can radically simplify the RX beamforming. Using this C-RX, an integrated scalable 730MHz 4-element C-RX phased array is fabricated using 65nm CMOS technology (Fig. 4). 7-bit programmable transconductor cells (g_m) are employed to convert each baseband (BB) node voltage in each C-RX into a corresponding current. Then, the current signals across all the elements are summed in the current domain in low-input impedance IQ transimpedance amplifiers (TIAs), implemented using two-stage op-amps. Therefore, the complex weights (phase shift and gain) applied to each element and the summation across all the elements are performed simultaneously while maintaining low noise and high linearity. Furthermore, the low input impedance combining point at the TIA input eases scalability across multiple chips. By connecting a second chip's low impedance node to the first one, and turning off the second chip's TIAs, the current from the g_m cells of the second chip can be combined into the TIAs of the first chip in the current domain. Thanks to the the low impedance provided by the TIA of the main chip, board trace capacitance does not degrade the performance in terms of BW.

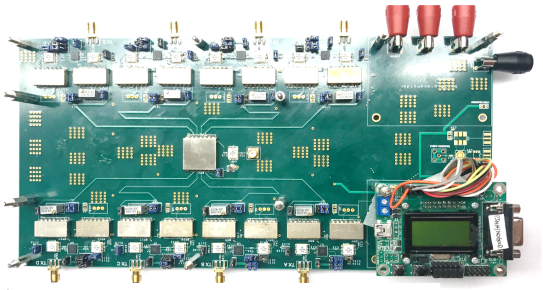
B. A Custom-Designed Transmitter Phased Array

Fig. 5 shows the custom-designed TX phased array, which is implemented using off-the-shelf discrete components.



Two 180 degrees phase-shifters has been used to provide full-360 degrees of phase-shift.

(a)



(b)

Fig. 5: A custom-designed 8-element transmitter phased array: (a) Block diagram, and (b) PCB implementation.

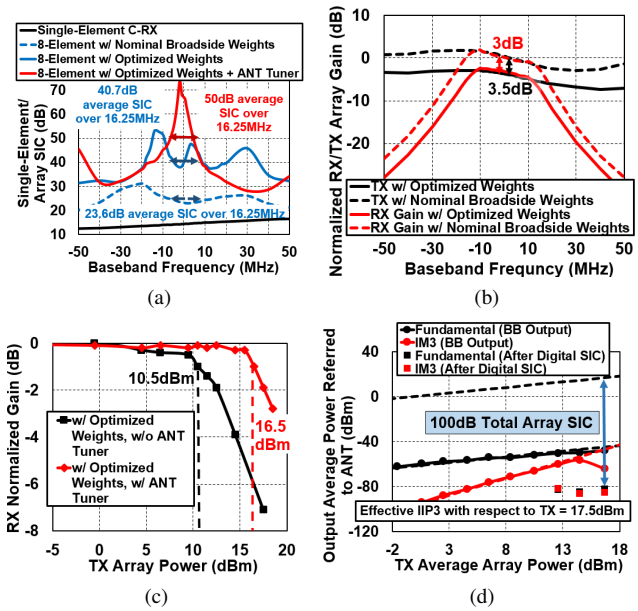


Fig. 6: Measured full-duplex phased array performance across 8-elements (tiling of 2 ICs): (a) array SIC, (b) impact of optimized weights to achieve SIC on the TX/RX array gain, (c) gain compression of a small received signal under the influence of TX power with optimized weights with and without the antenna tuner, and (d) two-tone TX test tracking the TX total SI and its IM3 products at the receiver output with additional digital SIC.

The signal is first amplified and divided into 8 channels using a Mini-circuits JCPS-8-10+ splitter. Each channel contains a cascade of two 180° phase shifters (Mini-circuits JSPHS-1000+) to cover the full 360° range, in series with multiple stages of a highly-linear low-noise amplifier (Mini-circuits HXG-122+) and a programmable attenuator to obtain amplitude control while maintaining good noise performance. The 7-bit attenuator (Skyworks SKY12343-364LF) provides a maximum attenuation of 31.75dB with 0.25dB resolution. System calculations show that the design can achieve upto 30dB gain with an output-referred IP_3 as high as 31dBm while the noise figure (NF) is less than 3.3dB.

C. Antenna Array

A rectangular 2×4 array is implemented using a slot loop antenna structure. The distance between adjacent elements is equal to half wavelength ($\lambda/2$). The antenna is fabricated on an FR-4 PCB and can radiate on both frontside and backside directions. A metal sheet is used as a reflector at the back of the antenna array with quarter wavelength distance to redirect the radiation to the frontside (Fig. 7).

D. Complete 8-element Full-duplex Phased array Transceiver

Two C-RX phased array ICs are tiled on a PCB to realize an 8-element FD C-RX phased array, which is then mounted on top of the TX phased array to form an 8-element FD phased array TRX with minimum interconnections (Fig. 7).

IV. Measurements and Demonstration

The single-element performance of the C-RX array is measured by turning ON only one element's g_m cells and shutting down all the other g_m cells. The C-RX shows 1.7dB TX-ANT loss, and +28dBm TX-ANT IIP_3. Although the nominal ANT-BB conversion gain is 41dB, this can go up to 50dB based on the programmable resistive feedback around the TIA. We also measured −31dBm/+22.5dBm in-band/out-of-band IIP_3 and 5dB single-element NF in the ANT-BB path due to the low-noise and high-linearity performance of the inverter-based g_m cells.

Array FD measurements are summarized in Fig. 6. The isolation of each C-RX element is around 15dB. When the TX and RX arrays are configured for nominal broadside beamforming, only an average of 23dB array SIC is achieved over 16.25MHz. Employing the optimization described in Section II, TX and RX DoF are repurposed to achieve SIC through beamforming while allowing 3dB TX and RX array gain loss, which leads to 40.7dB array SIC over 16.25MHz. The measured SIC profile is very wideband, and very similar to the simulated profile in Fig. 3. However, the achieved SIC is somewhat lower than simulation as the circulator's internal isolation and some second order effects such as quantization of beamforming weights are neglected in the simulations. Finally, custom-designed antenna tuners are integrated with antenna array. Co-optimizing the tuners (configured identically across all elements) with TX/RX weights leads to 50dB array SIC over 16.25MHz. The RX and TX array gain measurements verify the 3dB array gain loss versus frequency for broadside excitation as expected from the synthesized TX and RX array patterns for these weights (Fig. 3).

To evaluate array TX power handling when configured for SIC, a weak in-band signal is radiated towards the array and monitored while the TX array power ($P_{\mathrm{TX}} A G_{\mathrm{TX}}$) is swept. The 1dB desensitization of the C-RX array gain occurs at

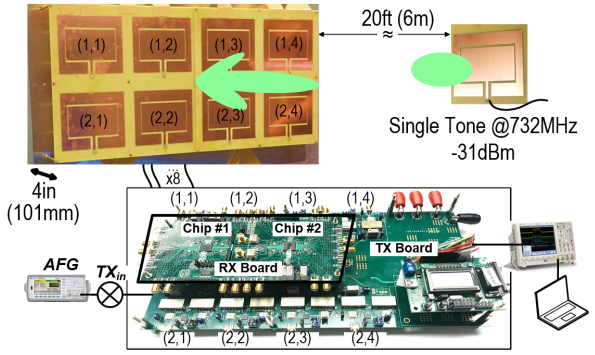


Fig. 7: Wireless FD demonstration setup.

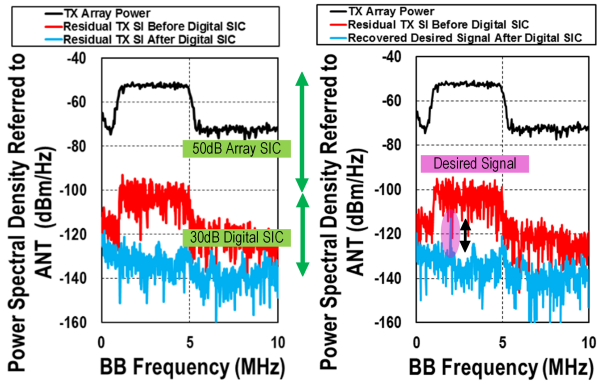


Fig. 8: Demo results: A -31dBm desired signal radiated from 20ft away from a single antenna is recovered while transmitting a 5MHz OFDM-like signal with $+8.7$dBm TX array power.

a TX array power of $+16.5$dBm. Finally, The effective IIP_3 referred to the TX array power is measured using a two-tone TX test while monitoring the RX IF outputs with weights configured for SIC. The effective IIP_3 referred to the TX array power is $+17.5$dBm. Nonlinear Volterra-series-based digital SIC at $+16.7$dBm average TX array power is able to suppress the residual total SI and its associated IM3 to below -84dBm, indicating 100dB total array SIC. However, an additional 19dB SIC is required to suppress the SI to the array noise floor (on the effective IIP_3 graph, the noise floor would be at $N_{\text{floor}}/AG_{\text{RX}} = -103$dBm), which can be potentially achieved with additional analog SIC.

We have successfully demonstrated around 80dB total self-interference cancellation for an OFDM-like signal with 10MHz RF bandwidth and a TX array average power of $+8.7$dBm , while simultaneously receiving a -31dBm continuous-wave desired signal radiating from a slot loop antenna placed 20ft away from the FD antenna array (Figs. 7, 8). This shows that the digital cancellation algorithm works effectively even when the desired signal is present.

V. Conclusion

In this work, phased array functionality is combined with full-duplex operation with no additional power consumption. Compared to the prior works, this works achieves higher total SI suppression, higher TX array power handling, and far superior potential FD link range (Table. II).

TABLE II: Comparison with state-of-the-art FD receivers with an integrated shared antenna interface.

		JSSC 2015 [6]	JSSC 2017 [7]	ISSCC 2017 [8]	This Work
	Architecture	Mixer-first TRX with Active Baseband Duplexing	RX with integrated magnetic-free N-path-filter-based circulator and BB SIC	Magnetic-free N-path-filter-based circulator-receiver with on-chip balance network	Full-duplex phased-array with integrated magnetic-free N-path-filter-based circulator-receivers
RX metrics	RX Frequency Range	0.1-1.5GHz	0.6-0.8GHz	0.61-0.975GHz	0.61-0.975GHz
	Number of Antenna Paths	1	1	1	**4 per IC, 2 ICs tiled for FD measurements**
	Gain	53dB	42dB	Max: 43dB Nominal: 28dB	Max: 51dB Nominal: 41dB (single-element)
	Noise Figure	5-8dB	8.4dB	6.3dB	5dB (single-element)
	OOB IIP3	+22.5dBm	+19dBm	+15.4dBm	+22.5dBm (single-element, 100MHz offset)
FD Metrics	Integrated SI Suppression Domains	Analog BB	RF + Analog BB	RF	**RF + Spatial**
	Amount of Integrated SI Suppression	33dB across 300kHz TX BB BW	42dB SIC across 12MHz BW	40dB SIC across 20MHz BW	**50dB array SIC across 16.25MHz BW (Across 8 elements)**
	Effective IIP3 with respect to TX Power	~0dBm at 43/53dB gain[1]	+1dBm at 42dB gain	+9dBm at 26dB gain	**+17.5dBm (TX Array Power)**
	Overall TX Port Power Handling	-17.3dBm[2]	-7dBm	+7dBm[2]	**+16.5dBm[2] (TX Array Power)**
	RX Degradation in Full-Duplex Mode	~2-5dB[3]	2.5dB	1.7dB	3dB (Array Gain Degradation)
	Overall SI Suppression	33dB	85dB (incl. digital SIC)	80dB (incl. digital SIC)	**100dB array SIC (incl. digital SIC)**
Resources	RX Power	43-56mW (incl. TX)	100mW signal path (10mW LO + 30mW BB canceller)	72mW	32mW for 4 elements on an IC
	Antenna Interface Power	Incl. in RX power	59mW (at 0.7GHz)	36mW (at 0.7GHz)	26.25mW per element
	Technology	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS
	Active Area	1.5mm^2	1.4mm^2	0.94mm^2	3.6mm^2 (0.9mm^2 / element)

1. From Fig. 31(a) in the paper. 2. Limited by ~1dB gain compression induced in the receive signal.
3. at -17.3dBm TX power.
N/A: Not Applicable N/R: Not Reported

VI. Acknowledgment

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