

# Poster: Enabling Wideband Full-Duplex Wireless via Frequency-Domain Equalization\*

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## ABSTRACT

Full-duplex (FD) wireless can significantly enhance spectrum efficiency but requires tremendous amount of self-interference (SI) cancellation. Recent advances in the RFIC community enabled wideband RF SI cancellation (SIC) in *integrated circuits (ICs)* via frequency-domain equalization (FDE), where reconfigurable RF filters are used to channelize the SI signal path. In [2], we designed and implemented an FDE-based RF canceller on a printed circuit board (PCB). We also presented an optimized canceller configuration scheme based on the derived canceller model, and extensively evaluated the performance of the FDE-based FD radios in a software-defined radio (SDR) testbed in different network settings.

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## 1 INTRODUCTION

Full-duplex (FD) wireless – simultaneous transmission and reception on the same frequency channel – can significantly improve spectrum efficiency at the physical (PHY) layer and provide many other benefits at the higher layers [7, 9]. The main challenge associated with FD is the extremely strong

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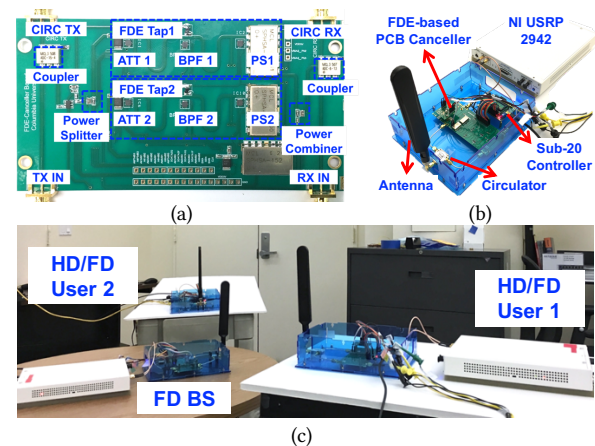


Figure 1: (a) The frequency-domain equalization- (FDE-) based wideband RF canceller implemented using discrete components on a PCB, (b) the implemented FDE-based FD radio, and (c) the experimental testbed consisting of an FD base station (BS) and 2 users that can operate in either half-duplex (HD) or FD mode.

self-interference (SI) signal that needs to be suppressed, requiring 90–110 dB of SI cancellation (SIC).

Recent work using off-the-shelf components and software-defined radios (SDRs) has established the feasibility of FD wireless through SI suppression at the antenna interface, and SIC in analog/RF and digital domains [1, 4, 5]. However, RF cancellers achieving wideband SIC (e.g., [1, 5]) rely on transmission-line delays, which cannot be realized in small-form-factor nodes and/or integrated circuits (ICs) due to the required length for generating nanosecond-scale time delays and the lossy nature of the silicon substrate.

A *compact IC-based* design is necessary for supporting FD in hand-held devices [8, 9]. Recent advances in the RFIC community allowed achieving wideband RF SIC in ICs based on the technique of frequency-domain equalization (FDE) [8]. In contrast to the delay line-based approaches (i.e., time-domain equalization), the FDE-based RF canceller utilizes reconfigurable 2<sup>nd</sup>-order bandpass filters (BPFs) with high quality factors to emulate the frequency-selective antenna interface. While major advances have been made at the IC level (e.g., [8]), there is still a need to: (i) understand the

fundamental limits of the achievable RF SIC based on the technique of FDE, (ii) develop efficient and adaptive configuration schemes for this new type of RF canceller, and (iii) evaluate the system-level performance of such IC-based FD radios in different network settings.

Since interfacing an RFIC canceller to an SDR presents numerous technical challenges, in [2], we designed and implemented an FDE-based RF canceller using discrete components on a printed circuit board (PCB). This *PCB canceller* (see Fig. 1(a)) emulates its RFIC counterpart and facilitates the evaluation of the canceller configuration scheme and experimentation in an SDR testbed with multiple FD nodes.

In this work, we present the design, implementation, and the optimized configuration scheme of the FDE-based RF canceller. We also perform experimental evaluation of the FDE-based FD radio at the link and network levels, demonstrating practical FD gains in different network settings.

## 2 FDE-BASED RF CANCELLER AND FD RADIO: DESIGN & IMPLEMENTATION

We briefly describe the FDE-based RF canceller, and the prototyped FD radios and testbed (for more details, please see [2]). **FDE PCB Canceller Implementation.** Fig. 1(a) shows the implemented PCB canceller with 2 FDE taps. In particular, a reference signal is tapped from the TX output and is split into two FDE taps. Then, the signals after each FDE tap are combined and RF SIC is performed at the RX input. Each FDE tap consists of a reconfigurable and high quality factor 2<sup>nd</sup>-order BPF (implemented and optimized around 900 MHz operating frequency), and an attenuator and phase shifter for amplitude and phase controls. The programmable attenuator has a tuning range of 0–15.5 dB with a 0.5 dB resolution, and the passive phase shifter is controlled by an 8-bit digital-to-analog converter (DAC) and covers full 360° range.

**FDE PCB Canceller Model.** To allow for efficient and adaptive canceller configuration, we derive a realistic model for the frequency response of the PCB canceller using the transmission (ABCD) matrix. This model is validated through extensive measurements and shown to have high accuracy.

**Optimized Canceller Configuration.** A general FDE-based canceller configuration scheme that jointly optimizes all the FDE taps is presented in [2] with inputs of: (i) the derived and validated PCB canceller model, (ii) the real-time antenna interface response (i.e., SI channel) measured using a preamble (2 OFDM symbols), and (iii) the desired RF SIC bandwidth. The canceller configuration scheme is implemented on the host PC, where the PCB canceller response is pre-computed and stored for computational efficiency. In particular, the PCB canceller configuration is obtained by solving an optimization problem followed by a finer-grained local search to achieve the best RF SIC performance.

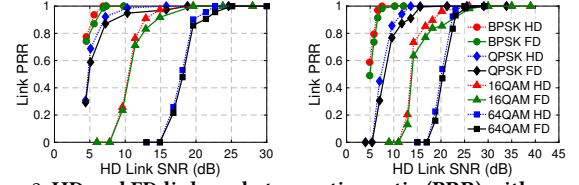


Figure 2: HD and FD link packet reception ratio (PRR) with varying HD link SNR and MCSs: (left) coding rate 1/2, (right) coding rate 3/4.

**FDE-based FD Radio and the SDR Testbed.** Figs. 1(b) and 1(c) depict our FDE-based FD radio design and the SDR testbed. A swivel blade antenna and a coaxial circulator are used as the antenna interface. We use the NI USRP-2942 SDR operating at 900 MHz carrier frequency, which is the same as the operating frequency of the PCB canceller.

We implemented a full OFDM-based PHY layer with a real-time RF bandwidth of 20 MHz using NI LabVIEW, supporting modulation and coding schemes (MCSs) with constellations from BPSK to 64QAM and coding rates of 1/2, 2/3, and 3/4. The digital SIC algorithm based on Volterra series with a highest non-linearity order of 7 is also implemented in LabVIEW to further suppress the residual SI signal after RF SIC.

Measurement results show that the FDE-based FD radio achieves an average 95 dB overall SIC across 20 MHz, from which 52 dB and 43 dB are obtained in the RF and digital domains, respectively. Since the USRP has a measured noise floor of −85 dBm (limited by the environmental interference at around 900 MHz), the FDE-based RF radio can support a maximum average TX power of +10 dBm (a peak TX power of 20 dBm). In total, our testbed consists of 3 FDE-based FD radios and regular USRPs without the PCB canceller.

## 3 EXPERIMENTAL EVALUATION

In this section, we present experimental evaluation of the FDE-based FD radios at the link and network levels.

**Link-Level: SNR-PRR Relationship and FD Gains.** We first evaluate the relationship between link SNR and packet reception ratio (PRR) using two FDE-based FD radios, where packets are sent over the link simultaneously in FD mode or in alternating directions in half-duplex (HD) mode (i.e., the two radios take turns and transmit to each other). In each experiment, both radios send a sequence of 50 OFDM streams, each OFDM stream contains 20 800-Byte OFDM packets.

Fig. 2 shows the relationship between link PRR and HD link SNR with varying MCSs. The results show that with sufficient link SNR values (e.g., 28 dB for 64QAM-3/4), the FDE-based FD radio achieves a link PRR of 100%. With insufficient link SNR values, the average FD link PRR is 6.5% lower than the HD link PRR across varying MCSs. Since packets are sent simultaneously in both directions on an FD link, this average PRR degradation is equivalent to an average FD link throughput gain of 1.87× under the same MCS.

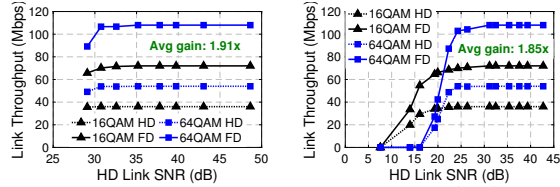


Figure 3: HD and FD link throughput in the LOS (left) and NLOS (right) experiments with 16QAM-3/4 and 64QAM-3/4 MCSs.

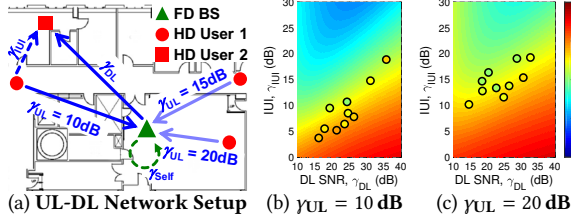


Figure 4: (a) Experimental setup for UL-DL networks, and (b)–(c) analytical (colored surface) and experimental (filled circles) network-level FD throughput gains with  $\gamma_{UL} = 10$  dB and  $\gamma_{UL} = 20$  dB.

We also conduct experiments in both line-of-sight (LOS) and non-line-of-sight (NLOS) settings on a 45 m  $\times$  20 m floor, and measure the HD (resp. FD) link throughput. The FD gain is computed as the ratio between FD and HD throughput values. Fig. 3 shows the average HD and FD link throughput with 16QAM-3/4 and 64QAM-3/4 MCSs. The results show that with sufficient link SNR values, the FDE-based FD radios achieve an *exact* link throughput gain of 2 $\times$  with a link PRR of 1. With medium link SNR values, where the link PRR less than 1, the average FD link throughput gains across varying MCSs are 1.91/1.85 $\times$  for the LOS/NLOS experiment.

**Network-Level FD Gains.** We experimentally evaluate the network-level FD throughput gains and compare to the analysis (e.g., [6]). We consider two types of networks: (i) *UL-DL networks* with one FD BS and two HD users with inter-user interference (IUI), and (ii) *heterogeneous HD-FD networks* with both HD and FD users. We apply a TDMA setting where each user equally shares the channel due to challenges in implementing a real-time MAC layer in software.

**UL-DL Networks with IUI.** Fig. 4 shows the analytical (colored surface) and experimental (filled circles) FD gains. It can be seen that smaller values of  $\gamma_{UL}$  and lower ratios between  $\gamma_{DL}$  and  $\gamma_{UL}$  lead to higher FD gains in both analysis and experiments, and the average experimental FD gains are 1.25/1.16/1.14 $\times$  for  $\gamma_{UL} = 10/15/20$  dB. Overall, the average experimental FD gain is 93% of the analytical FD gain. The results confirm the analysis in [6] and demonstrate practical FD gains in wideband UL-DL networks without changing the current network stack (i.e., only bringing FD capability to the BS). Moreover, performance improvements are expected through advanced power control and scheduling schemes.

**Heterogeneous 4-Node Networks.** We also experimentally study 4-node networks (e.g., see Fig. 5(a)) where zero,

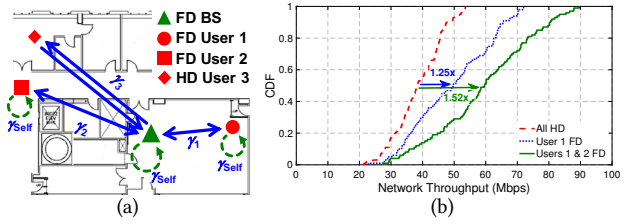


Figure 5: (a) Experimental setup for heterogeneous 4-node networks, and (b) CDF of experimental network-level FD throughput gains when zero, one, or two users are FD-capable.

one, and two users are FD-capable. Fig. 5(b) shows the CDF of the experimental FD throughput gains with measured link SNR between 5–45 dB. Overall, the median network throughput is increased by 1.25/1.52 $\times$  when one/two users become FD-capable. The trend shows that in real-world environments, the network throughput increases as more users become FD-capable, and the improvement is more significant with higher user SNR values. Note that we only apply a TDMA scheme and a more advanced MAC layer (e.g., [3]) has the potential to improve the FD gains in these networks.

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