A Survey and Quantitative Evaluation of Integrated Circuit-based Antenna Interfaces and Self-Interference Cancellers for Full-Duplex

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Full-duplex (FD) wireless – simultaneous transmission and reception on the same frequency – is a promising technique that can significantly improve spectrum efficiency and reduce communication latency in future wireless networks. To enable FD operation, the powerful self-interference (SI) signal leaking from the transmitter (TX) into the receiver (RX) needs to be suppressed and canceled to an extreme degree at the antenna interface as well as in the RF/analog and digital domains. Various approaches to achieve TX-RX isolation at the antenna interface and SI cancellation (SIC) in the RF/analog and digital domains have been demonstrated, with a focus on using bench-top off-the-shelf components. Recent advances in integrated circuit (IC) implementations of various types of shared antenna interfaces and cancellers in the RF and/or analog baseband (BB) domains have further pushed the frontier of realizing FD wireless in small-form-factor/hand-held devices. Moreover, it is still important to fundamentally study the SIC performance that can be achieved by different types of cancellers. In this paper, we present a first-of-its-kind comprehensive overview on the implementation and comparison of various state-of-the-art *integrated shared antenna interfaces and SI cancellers in both the RF and analog BB domains*. We define two figures of merit (FOM) for the IC-based shared antenna interfaces and SI cancellers, which capture various design considerations and performance tradeoffs including the achievable isolation/SIC, bandwidth, noise figure degradation, TX/SI power handling, and power consumption. In particular, we focus on two types of integrated shared antenna interfaces including electrical-balance duplexers and circulators. We also discuss two types of SI cancellers based on the time-domain and frequency-domain approaches, which respectively employ parallel delay lines and bandpass filters to emulate the SI channel. Based on realistic measurements, we perform extensive numerical evaluations to illustrate and compare the achievable RF SIC performance in different scenarios, as well as discuss various design tradeoffs. Finally, we provide an overview of the IC-based implementations and performance evaluations of both types of cancellers based on our recent work.

***Index Terms*—Full-duplex wireless, integrated circuit (IC), antenna interface, self-interference cancellation, systems and testbeds**

I. Introduction

Existing wireless systems such as Wi-Fi and cellular networks operate in half-duplex mode, where radios transmit and receive in different time slots (i.e., time-division duplexing, TDD) or frequency channels (i.e., frequency-division duplexing, FDD). Full-duplex (FD) wireless is an emerging communication paradigm that supports simultaneous transmission and reception of radio signals at the same frequency [2]–[5], therefore providing many benefits such as improved spectrum efficiency and data rates, and reduced communication latency. However, one of the fundamental challenges associated with enabling FD wireless is the strong self-interference (SI) signal that leaks from a radio's transmitter (TX) into its receiver (RX), which is usually at least a billion times (i.e., >90 dB) stronger than the desired signal. Therefore, powerful multi-stage SI cancellation (SIC) is required across the propagation (e.g., at the antenna interface), RF/analog, and digital domains (for details see [2], [5]–[14] and the references therein).

Various approaches to achieve SI suppression/cancellation in the propagation domain as well as SIC in the RF/analog and digital domain have been extensively studied and summarized in overview papers [2], [10], [11] with a focus on bench-top implementations using commercial off-the-shelf (COTS) components. In recent years, there have been extensive advances in integrated circuit (IC) implementations of critical components for an FD radio, including shared antenna interface and SI canceller circuitry. These components and their performance are crucial for realizing FD wireless in mobile/hand-held devices such as laptops and cell phones. In addition, despite a large number of SI canceller implementations in both ICs and on printed circuit boards (PCBs), a fundamental understanding of the various design tradeoffs of SI cancellers with different degrees of reconfigurablility is still lacking.

In the first part of this paper, we focus on *integrated shared antenna interface* and *integrated SI cancellers in the RF and analog baseband (BB) domains* (see Fig. 1), which can provide TX-RX isolation and SIC, respectively, and thus largely alleviate the dynamic range requirements at the RX. We present a comprehensive overview of recent advances in novel and practical IC-based shared antenna interface and canceller implementations. In particular, we consider two popular approaches for integrated shared antenna interfaces: an *electrical-balance duplexer (EBD)*, which is a reciprocal four-port passive device [15]–[23], and a *circulator*, which is a non-reciprocal three-port component [24]–[40]. For quantitative and fair comparison, we define two figures of merit (FOM): (i) the *antenna interface efficiency*, which captures the tradeoffs between various performance metrics including the TX power handling, TX-ANT loss, RX noise figure (NF) degradation, and the DC power consumption, and (ii) the *isolation-fractional bandwidth (FBW) product*, which captures

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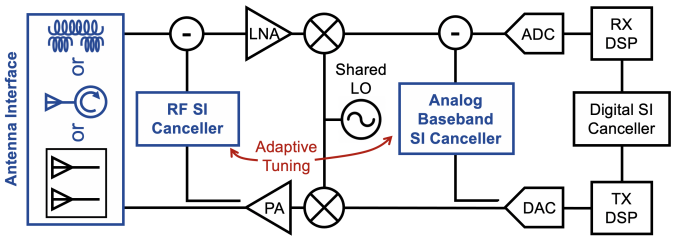

Fig. 1: Block diagram of a full-duplex (FD) radio, where the highlighted blocks (i.e., circulator, electrical-balance duplexer [EBD], RF and analog baseband [BB] SI canceller) and their integrated circuit (IC) implementations are the focus of this paper.

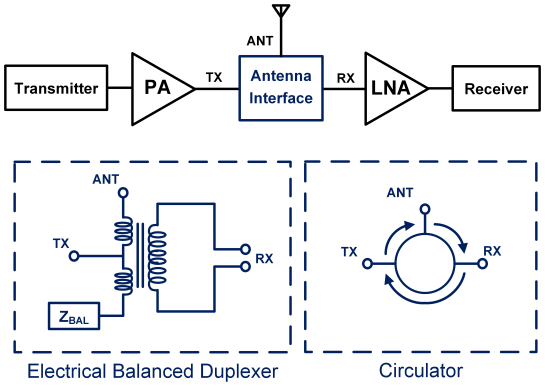

Fig. 2: Block diagram of a transceiver with a shared antenna interface using an electrical balanced duplexer (EBD) or a circulator.

the amount of achievable isolation and the FBW with which the antenna interfaces can operate.

To suppress the SI even further, in the RF and/or analog BB domains, a reference signal is tapped from the TX output and passed through the *SI canceller*, and SIC is performed at the RX input (see Fig. 1). We present a detailed overview of two types of SI cancellers using different approaches: (i) *time-domain* cancellers (in the RF and/or analog BB domains) employing parallel delay line (DL) taps, and (ii) *frequency-domain* cancellers (in the RF domain) employing parallel RF bandpass filter (BPF) taps. Although both types of cancellers have been realized and demonstrated in practical systems (e.g., [7], [41]–[43]), we focus on their recent implementations in ICs [15], [16], [28], [29], [38], [39], [44]–[70]. For quantitative and fair comparison similar to the integrated antenna interfaces, we define two FOM for integrated cancellers: (i) the *canceller efficiency*, and (ii) the *SIC-FBW product*.

In the second part of the paper, we provide an overview of two adaptive canceller tuning algorithms based on the *minimum mean square error (MMSE)* and *dithered linear search (DLS)* methods, which are important since an SI canceller with reconfigurable parameters needs to be configured in an adaptive and efficient manner to achieve optimized SIC performance. Then, we numerically evaluate the performance of different RF cancellers with different settings (e.g., number of DL/BPF taps) under varying antenna interfaces, desired SIC bandwidth, and with and without practical hardware quantization constraints. The evaluation results illustrate the relationship between these factors and the corresponding achievable RF SIC in different scenarios. We believe that these results can provide insights into RF canceller designs with different hardware constraints and performance requirements.

Finally, based on our recent work, we present an overview of one IC-based time-domain canceller integrating reconfigurable RF and analog BB taps [44], and a frequency-domain RF canceller implemented both in an IC and on a PCB [43], [66]. The frequency-domain RF cancellers are also integrated with a software-defined radios (SDR) platform to prototype complete FD radios. These FD radio are integrated in the open-access city-scale NSF PAWR COSMOS advanced wireless testbed [71] together with open-source software and example experiments to facilitate research in the area of FD wireless.

To summarize, the main contributions of this paper are: (i) *a comprehensive overview of various state-of-the-art integrated shared antenna interface and canceller implementations, and the comparison of their key performance metrics based on two FOM*, (ii) *extensive measurement-based numerical evaluations* which, to the best of our knowledge, are the first attempt towards a fundamental understanding of the design tradeoffs in different types of cancellers with varying parameters. Note that while there has also been extensive recent work on analyzing benefits introduced by FD in terms of the link budget and rate gain at the link/network level (e.g., [6], [72]–[74] and the references in [2]), the focus of this paper is on the key components of and recent advances in integrated FD radios.

The rest of this paper is organized as follows. We start with the overview and comparison of recent integrated shared antenna interface implementations in Section II. In Section III, we describe two SI canceller models based on the time- and frequency-domain approaches. Then, in Section IV, we present the overview and comparison of recent integrated SI canceller implementations. Two different canceller configuration algorithms are presented in Section V. In Sections VI and VII, we present numerical evaluations of different cancellers in realistic scenarios and provide an overview of our recent hardware implementations, respectively. We conclude with open challenges and future directions in Section VIII.

II. Integrated Shared Antenna Interfaces for Full-Duplex Systems

One critical component for realizing compact, low cost integrated FD radios is an *integrated shared antenna interface* (see Fig. 1) that can provide the first stage of SI suppression and avoids RX saturation. An ideal antenna interface should be able to provide a sufficient amount of TX-RX isolation with high TX power handling and linearity performance, low loss in the TX to ANT path, and low noise figure (NF) in the ANT to RX path. It also needs to adapt to variations in the environment to preserve the achievable TX-RX isolation. Obtaining a high isolation from the antenna interface reduces the amount of SIC required by the RF, analog BB, and digital domains. This also reduces the dynamic range requirement of the analog (RF and BB) cancellers which can be exploited to realize cancellers with lower power consumption and/or lower noise figure (NF). Below, we focus on recent IC implementations

of two common shared antenna interfaces: *electrical-balance duplexers (EBDs)* [15]–[23], and *circulators* [24]–[40]. Table I provides a summary and comparison of performance for these antenna interfaces.

A. Integrated Electrical-Balance Duplexers (EBDs)

An EBD is a *reciprocal four-port passive device*, in which three ports are connected to the TX, RX, and antenna ports, and the fourth port is terminated by a balance network, whose impedance can be tuned to balance the antenna's impedance to provide isolation between the TX and RX ports. As shown in Fig. 2, a typical EBD utilizes a hybrid transformer: the TX output is connected to the center tap of the primary coil, whose end terminals are connected to the antenna and a balancing load, respectively, and the RX input is connected differentially to the two terminals of the secondary coil. If the load balance network impedance matches the antenna impedance (i.e., $Z_{\text{BAL}} = Z_{\text{ANT}}$), then the signal from the TX appears across the two terminals in the RX port as a common mode signal whereas the signal from the antenna appears as a differential mode signal. Thus, using a differential RX provides isolation between the TX and RX ports. However, the signal from TX-to-ANT and ANT-to-RX experiences a theoretical loss of 3 dB due to the reciprocal nature of the EBD, which is equivalent to having a 3 dB lower transmit power (P_{TX}), and a 3 dB degradation in the receiver NF. In addition, a practical EBD implementation usually exhibits a higher loss (e.g., 3.7 dB in [21], 5.6 dB in [16], and 5–6 dB in [15]). Due to the passive nature of these balancing impedance networks, EBDs do not consume any DC power. and can support very high TX power handling which is only limited by the switches used in the isolation tuning network.

As shown in Fig. 2, some of the early EBD implementations utilized a floating differential RX port, thus requiring an additional balun when using a single-ended LNA. In [22], [23], a multi-band EBD with a modified architecture using a single-ended RX port was demonstrated, where >40 dB isolation is achieved across 180 MHz bandwidth using an RC balancing network, which supports an antenna impedance of up to 1.5:1 voltage standing wave ratio (VSWR). Moreover, this EBD achieves a TX power handling of up to +22 dBm.

In [20], [21], an EBD achieving a very high linearity of +70 dBm IIP3 was demonstrated, which meets the stringent requirements of modern wireless standards (e.g., a 3GPP test scenario with a −15 dBm out-of-band jammer intermodulating with a +27 dBm TX signal). It uses a single-ended RX port by grounding one of the terminals in the secondary winding which allows the use of a single-ended LNA at the RX input. The balancing network in this work was implemented using an RLC network with four 8-bit tunable capacitors to achieve >50 dB isolation across 300 MHz bandwidth, supporting an antenna impedance of up to 1.5:1 VSWR. These capacitor values are optimized on an FPGA to find the optimal solution in less than 1 ms [82]. In order to obtain high linearity and high power handling levels, the tuning switches are built by stacking four SOI CMOS transistors so that each of them sees a smaller portion of the voltage swing, supporting TX power levels up to +27 dBm. EBDs have also been demonstrated at mmWave frequencies along with an on-chip bow-tie antenna (e.g., at 120 GHz [18], [19]) which supports an antenna impedance ranging between $92-j34\,\Omega$ and $45-j5\,\Omega$. Using polyresistors and NMOS transistors in parallel for the balancing network, >30 dB isolation can be achieved across 14 GHz bandwidth. In addition, integrated EBDs along with separate cancellers to realize a complete FD transceiver have been demonstrated in [16] and [15], where 39/30 dB isolation across 200/500 MHz bandwidth (both at 1.75 GHz operating frequency) is achieved, respectively.

B. Integrated Circulators

A circulator is a *non-reciprocal three-port component*, where the signal incident at any port "circulates" in a single direction (i.e., clockwise or counter-clockwise), as shown in Fig. 2. For an ideal circulator, the power incident at any port will be completely transferred to another port and remains isolated from the third port. This isolation can be used to suppress the SI from the TX to the RX while maintaining the signal transfer from the TX to the antenna as well as from the antenna to the RX. Therefore, connecting the TX, RX, and antenna ports of a radio to the three ports of a circulator can provide TX-RX isolation between the TX and RX ports without introducing losses in the signal paths between TX-ANT and ANT-RX, by virtue of the non-reciprocal nature of the circulator. Unlike EBDs, a circulator theoretically has no loss and therefore does not lead to degradation in transmit power and RX NF. While there have been several non-IC-based circulator implementations [83]–[89], in this paper we focus specifically on recent IC-based circulator implementations. For a more comprehensive overview on different (both integrated and non-integrated) circulator implementations, we refer the reader to [90].

Traditionally, circulators are implemented using ferrite materials which lose reciprocity in the presence of an external magnetic field. Fabrication of these ferrite materials requires high deposition temperatures rendering them incompatible with semiconductor fabrication, therefore leading to bulky size and high implementation cost. Another approach is to use active components to achieve non-reciprocity and realize circulators [40], [91]–[93]. However, these implementations suffer from poor linearity and noise performance in the presence of very high TX power levels [94]. Furthermore, non-idealities such as clock feed-through, thermal noise, and distortion exist even in passive CMOS implementations. Since most works do not report these metrics explicitly, we use the NF degradation and TX power handling as the metrics for the noise and distortion performance, respectively.

Recent research has demonstrated promising IC-based circulator implementations using switch-based spatio-temporal conductivity modulation through networks known as N-path filters [95]. In particular, two-port N-path filters can achieve phase non-reciprocity by staggering the clocks of the two sets of switches, which results in signal transmission with non-reciprocal phase response ($+90°/-90°$ in the forward/reverse direction) and realizes a CMOS gyrator. Then, a $3\lambda/4$ transmission line can be wrapped around this gyrator to achieve

TABLE I: Summary and comparison of IC-based antenna interface implementations.

Work	Category	Operating Frequency	TX-RX Isolation	Power Consumption	ANT-RX Noise Figure	TX-ANT Loss	TX Power Handling	Technology/ Area	Efficienc	ISO-FBW Product
ISSCC'20 [24], JSSC'20 [25]	Circulator	0.914–1.086 GHz	>40 dB/92 MHz, >25 dB/172 MHz @1 GHz	39 mW	2.5 dB	−2.07 dB	34 dBm	180 nm/ 9 mm^2	27.6%	>29.6 dB
JSSC'20 [75]	Circulator	5.6–7.4 GHz	>18 dB/1.82 GHz @6.5 GHz	2.5 mW	2.4–3.4 dB	-2.2 dB	N/A	40 nm/ 0.45 mm^2	N/C	12.5 dB
RFIC'20 [76]	Quadrature Coupler	1.5–3 GHz	10–26 dB/1 GHz @2.25 GHz	N/A	1.9 dB[(i)]	−3.6 dB	21 dBm	65 nm/ 1.6 mm^2	22.4%	22.5 dB
RFIC'20 [26]	Circulator	DC–1 GHz	>18 dB/1 GHz @0.5 GHz	20 mW	3.1–4.1 dB	−3.1 dB	1.4 dBm	65 nm/ 0.19 mm^2	3.6%	>21.0 dB
RFIC'20 [77]	Bi-direct. Frequency Converter	3.4–4.6 GHz	25.5 dB/1.2 GHz @4 GHz	48 mW	5.8 dB (w/ RX down-conversion)	−3.0 dB	21 dBm	65 nm/ 0.27 mm^2	N/C	20.3 dB
IMS'20 [15]	EBD	1.5–2 GHz	30 dB/500 MHz @1.75 GHz	0 mW, passive	6 dB	−5.0 dB	10 dBm	65 nm/ 1.5 mm^2	6.3%	24.6 dB
ISSCC'19 [27]	Circulator	50–56.8 GHz	>20 dB/6.8 GHz, >40 dB/1.3 GHz @53.4 GHz	24.14 mW	3.2 dB	−3.6 dB	19.65 dBm	45 nm/ 1.72 mm^2	15.4%	>23.9 dB
ISSCC'19 [28], JSSC'19 [29]	Circulator	2.2 GHz	15 dB/40 MHz @2.2 GHz	156 mW	N/A	−3.7 dB	14 dBm	65 nm/ 2.2 mm^2 per element	8.4%	-2.4 dB
JSSC'19 [30]	Circulator	90/100/105 GHz	46–47 dB/1.5 GHz @100 GHz	17.3–18.6 mW @100 GHz	5.2 dB	−5.6 dB	11.4 dBm	65 nm/ 0.21 mm^2	4.2%	28.8 dB
TMTT'19 [31]	Circulator	0.91 GHz	>20 dB/20 MHz @0.91 GHz	64 mW	5.2 dB	−4.8 dB	N/A	65 nm/ 36 mm^2	N/C	>3.4 dB
IMS'19 [32]	Circulator	0.1–1 GHz	>18 dB/900 MHz @0.55 GHz	4.1 W	3.0 dB	−3.0 dB	N/A	0.2 μm GaN/ 18.5 mm^2	N/C	20.1 dB
ISSCC'18 [33]	Circulator	0.55–0.9 GHz	40 dB/56 MHz, >30 dB/190 MHz @0.8 GHz	24 mW	2.7 dB	−2.6 dB	5.5 dBm	65 nm/ 38.6 mm^2	7.7%	>23.8 dB
ISSCC'18 [16]	EBD	1.6–1.9 GHz	39 dB/200 MHz @1.85 GHz	0 mW, passive	5.6 dB	N/A	N/A	40 nm/ 4 mm^2	N/C	29.6 dB
ISSCC'18 [53], JSSC'18 [54]	Multi-feed Antenna	60–75 GHz	>35 dB/15 GHz @67.5 GHz	0 mW, passive	0.52 dB[(i)]	−1.1 dB	10.5 dBm	45 nm/ 7.3 mm^2	54.7%	>28.5 dB
RFIC'18 [34], JSSC'19 [35]	Circulator	0.86–1.08 GHz	>25 dB/161 MHz @1 GHz	170 mW	3.1 dB	−2.1 dB	30.66 dBm	180 nm/ 16.5 mm^2	23.0%	>17.2 dB
CICC'18 [17]	EBD	1.1–2.5 GHz	31 dB/40 MHz @1.8 GHz	0 mW, passive	N/A	N/A	15 dBm	45 nm/ 1.4 mm^2	N/C	14.5 dB
ISSCC'17 [36], JSSC'17 [37]	Circulator	25 GHz	>18.5 dB/4.5 GHz @ 25 GHz	78.4 mW	3.3–4.4 dB	−3.3 dB	21.5 dBm	40 nm/ 2.16 mm^2	14.9%	>11.1 dB
ESSCIRC'17 [18], JSSC'16 [19]	EBD	120 GHz	>30 dB/14 GHz @ 120 GHz	0 mW, passive	<12 dB[(i)]	−11.0 dB	N/A	40 nm/ 0.015 mm^2	N/C	>10.7 dB
ISSCC'16 [38], JSSC'17 [39]	Circulator	610–850 MHz	20 dB/12 MHz @730 MHz	59 mW	4.3 dB	−1.7 dB	7 dBm	65 nm/ 1.4 mm^2	4.4%	2.2 dB
RFIC'16 [78], JSSC'17 [79]	Distributed PA-based duplexer	0.3–1.6 GHz	>25 dB/N/R @900 MHz	0 mW, passive	4–5 dB	0.0 dB	14 dBm	65 nm/ 7.2 mm^2	31.6%[(ii)]	N/C
ISSCC'15 [20], TMTT'16 [21]	EBD	1.9–2.2 GHz	>50 dB/>200 MHz @1.95 GHz	0 mW, passive	<3.7 dB[(i)]	−3.7 dB	27 dBm	180 nm/ 1.75 mm^2	14.5%	>39.9 dB
RFIC'14 [80], JSSC'15 [81]	Duplexing LNA	0.1–1.5 GHz	30 dB/N/A @0.8 GHz	43–56 mW (Total TX and RX power)	0 dB (RX NF)	N/A	N/A	65 nm/ 1.5 mm^2	N/C	N/C
TMTT'14 [40]	Circulator	62–75 GHz	18 dB/13 GHz @68.5 GHz	N/A	N/A	−7.4 dB	N/A	45 nm/ 1.24 mm^2	N/C	10.8 dB
CICC'14 [22], TMTT'16 [23]	EBD	1.6–2.2 GHz	>40 dB/180 MHz @1.9 GHz	0 mW, passive	N/A	−3.2 dB	22 dBm	180 nm/ 0.35 mm^2	N/C	>29.8 dB

[(i)] Obtained from the ANT-RX insertion loss of the antenna interface.
[(ii)] Distributed PA architectures have lower efficiency which is not being considered here.
[(iii)] NF: Noise Figure; ISO-FBW Product: Isolation-Fractional Bandwidth (FBW) Product (see (2) in Section II-D).
[(iv)] N/A: Not Available/Applicable, i.e., metric was not reported in the specific implementation. N/C: Not Computable.

signal propagation in a single direction, and connecting the three ports with a spacing of $\lambda/4$ on the transmission line realizes a three-port circulator. The linearity of the circulator for FD wireless can be optimized by placing the gyrator close to the RX port, which suppresses the voltage swings across the gyrator due to an excitation at the TX port.

Using this technique, [38], [39] demonstrated a CMOS circulator that achieves 20 dB isolation across 12 MHz bandwidth with an antenna whose impedance is tuned using an off-chip impedance tuner to maximize the reverse isolation at

the center frequency. N-path filters require low duty cycle clocks thereby requiring high frequency transistors which typically offer lower power handling. Additionally, extending these approaches to millimeter-wave (mmWave) frequencies is challenging due to the complex clocking requirement. As an alternative, switched transmission line based structures were proposed to realize non-reciprocal gyrator elements and these structures require 50% duty cycle clocks at sub-harmonics of the operating frequency, thereby enabling the usage of "slower" transistors with high power handling [96], [97]. Clocking the switches at the n-th sub-harmonic of the operating frequency enables operation at n times higher frequency compared to N-path filters. These approaches have been leveraged to realize mmWave circulators. By using C-L-C sections to realize transmission lines in the gyrator, >18.5 dB isolation can be achieved across 4.5 GHz bandwidth at 25 GHz [36], [37] with a 50 Ω load used for the antenna (with 8.3 GHz clocking frequency of the switches). For operation in similar frequency ranges, N-path filter based implementations would require clocking at 25 GHz which is impractical using current CMOS technologies. This implementation also has an increased fractional bandwidth of 18% which is around 4× higher than the N-path filter based implementation. In addition, the operating frequency can be further enhanced by using bandpass filters instead of transmission lines, as they can absorb larger switch parasitics and enables circulators with low loss. For example, a CMOS circulator that achieves >20 dB isolation across 6.8 GHz bandwidth at 53.4 GHz (with 8.6 GHz clocking frequency of the switches) was demonstrated in [27].

Using a similar gyrator architecture at RF can help reduce the clocking frequency which enables usage of high voltage transistors that provide high TX power handling. Adding other linearity enhancement techniques such as device stacking and optimal switch biasing, a CMOS circulator handling >1 W (>30 dBm) TX power has been demonstrated in [34], [35], which represents a 10–100× enhancement in linearity and TX power handling compared to [37], [39]. Low-loss inductor-free antenna balancing techniques have also been implemented to account for the antenna impedance variation due to environmental reflections using feed-forward cancellation paths to achieve >25 dB isolation across 161 MHz bandwidth for a wide range of antenna impedance up to a VSWR of 1.85.

Later, using special clocking schemes such as switched-capacitor clock boosting, the TX power handling of these circulators was further enhanced to 2.5 W. By lowering the characteristic impedance of the transmission line in the gyrator and using periodically loaded inductors to realize transmission lines, both the chip area and power consumption of the circulator can be largely reduced. Using these techniques, an integrated circulator that achieves >40 dB isolation across 92 MHz bandwidth for a wide range of antenna impedance up to a VSWR of 2.33 was presented in [24], [25]. Similar architectures of switched-transmission lines have been implemented in gallium nitride (GaN) technologies to realize ultra-wideband circulators [32]. By replacing the $3\lambda/4$ transmission line around the N-path filter with a hybrid coupler, a circulator-receiver with enhanced bandwidth has been realized in [33]. This architecture has been shown to provide >30 dB isolation across 190 MHz bandwidth for a wide range of antenna impedances up to a VSWR of 1.35 without an on-chip balancing network. Recently, an ultra-wideband IC-based circulator operating from DC–1 GHz has also been demonstrated by utilizing a new regime in N-path switched-capacitor networks, which enables ultra-broadband, ultra-compact, and non-reciprocal true-time-delay elements [26], where >18 dB isolation is achieved across the entire bandwidth of DC–1 GHz with a 50 Ω termination at the antenna port.

C. Other Integrated Shared Antenna Interfaces

Apart from the EBDs and circulators described above, there are other techniques to obtain TX-RX isolation using a shared antenna interface. One such approach is using a multi-feed slot-loop antenna with two TX feeds and two RX feeds [53], where the TX feeds are driven differentially to synthesize a standing-wave voltage distribution on the slot loop. The RX feeds are placed such that the TX signals have voltage nulls at the location of the RX feeds, thus providing isolation between TX and RX. The prototype using this technique demonstrated >35 dB TX-RX isolation between 60–75 GHz.

In [76], a digital transmitter based on quadrature balanced switched-capacitor power amplifiers has been demonstrated to achieve isolation between the TX and RX. Here, two PAs operating at 90° phase offset are combined through a quadrature coupler, which results in the TX signal interfering constructively at the antenna port and destructively at the RX port thereby providing isolation between the TX and RX. This provides an isolation of 10–26 dB across 1 GHz bandwidth.

Frequency translation can also be used to realize shared-antenna interfaces [77]. In this work, a bi-directional frequency converter (BDFC) realizes a direction independent down-converter that enables splitting the TX and RX frequencies on chip, which can be later decoupled by using respective frequency selective filters. Using this technique, 25.5 dB isolation has been demonstrated between 3.4–4.6 GHz.

In [78], [79], the antenna is connected to the RX using multiple artificial transmission line segments in series. The PA is distributed into multiple sub-PAs and each of the sub-PAs is connected to the nodes in between the transmission line segments. Each of the sub-PAs has a separate gain and phase control which can be tuned such that the TX signals add constructively at the antenna and destructively at the receiver, thus providing isolation. Received signals from the antenna directly propagate to the receiver through the transmission lines. The prototype using this technique provides an isolation of >25 dB from 0.3–1.6 GHz.

In addition, unlike typical shared antenna interfaces that operate at RF, duplexing operation for enabling FD wireless has been demonstrated at baseband frequencies [80], [81]. This approach utilizes a passive mixer-first architecture sharing a single passive mixer to perform simultaneous up-conversion and down-conversion. The duplexing operation can be implemented in the baseband due to the bi-directional transparency of the passive mixer. A prototype using this technique was presented in [80], [81], which demonstrates 30 dB isolation at 0.8 GHz operating frequency.

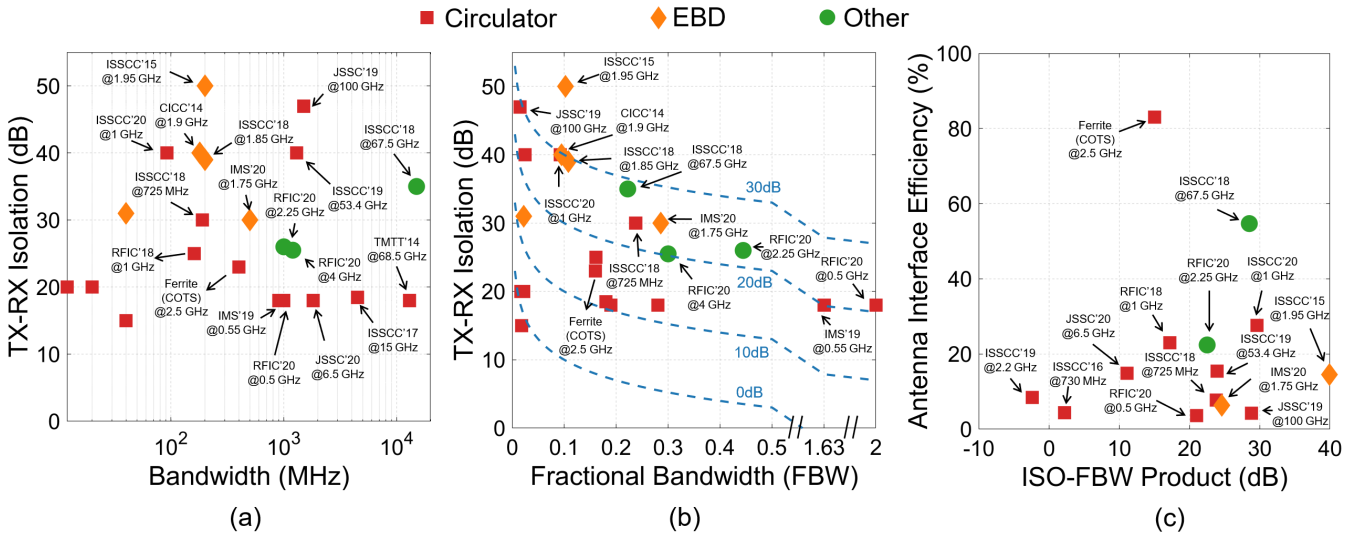

Fig. 3: TX-RX isolation achieved by various integrated shared antenna interfaces as a function of the (a) isolation bandwidth and (b) fractional bandwidth (with contours indicating constant isolation fractional bandwidth product). (c) Antenna interface efficiency achieved by various integrated shared antenna interfaces as a function of the isolation fractional bandwidth product.

D. Comparison and Figure of Merit (FOM)

Table I summarizes the comparison between different state-of-the-art antenna interfaces. An ideal antenna interface must provide high isolation across a large bandwidth relative to the center frequency, and handle large TX power while adding low noise or equivalently having low loss. However, these metrics tradeoff with each other in realistic IC implementations.

To provide a comprehensive and fair comparison between the shared antenna interfaces, we discuss two figures of merit (FOM): (i) *antenna interface efficiency*, denoted by η_{ANT}, which evaluates the degradation in the power-amplifier efficiency due to the presence of the antenna interface by taking into account its TX power handling, TX-ANT insertion loss, RX noise figure (NF) degradation, and DC power consumption [90], [98], and (ii) *isolation-fractional bandwidth product*, where the fractional bandwidth (FBW) is the ratio of the bandwidth of isolation and the center frequency.

1) Antenna Interface Efficiency

The antenna interface efficiency (η_{ANT}) evaluates the degradation in the power amplifier (PA) efficiency due to the presence of additional circuitry to enable FD communication with a shared antenna. We consider an FD wireless link consisting of a PA generating a total output power $P_{\text{out,PA}}$ with a drain efficiency of η_{PA} and an antenna interface with TX-ANT insertion loss of $L_{\text{TX-ANT,ANT-INT}}$, ANT-RX NF of $NF_{\text{ANT-INT}}$, and DC power consumption $P_{\text{DC,ANT-INT}}$. The effective transmitted power of the wireless link relative to that of an ideal antenna interface with no added loss or NF can be expressed as

$$P_{\text{out,link}} = P_{\text{out,PA}} \times L_{\text{TX-ANT,ANT-INT}}/NF_{\text{ANT-INT}}.$$

The total DC power consumption on the transmit side will be the sum of the PA's DC power consumption, $P_{\text{DC,PA}}$, and the antenna interface's DC power consumption, $P_{\text{DC,ANT-INT}}$. (assuming that the RX DC power consumption is negligible compared to the TX). The PA's DC power consumption can be computed from the total output power and its efficiency as $P_{\text{DC,PA}} = P_{\text{out,PA}}/\eta_{\text{PA}}$. The efficiency of the antenna interface can be expressed as the ratio between the effective transmitted power and the total DC power consumption normalized to the PA's efficiency:

$$\eta_{\text{ANT}} = \frac{P_{\text{out,PA}} \times L_{\text{TX-ANT,ANT-INT}}/NF_{\text{ANT-INT}}}{P_{\text{out,PA}}/\eta_{\text{PA}} + P_{\text{DC,ANT-INT}}} \times \frac{1}{\eta_{\text{PA}}} \times 100\%. \tag{1}$$

In a practical system, the maximum value of $P_{\text{out,PA}}$ is limited by the maximum TX power handling of the antenna interface which is determined by the TX power at which the TX-ANT transmission compresses by 1 dB, i.e., the TX-ANT P1dB. We also add 1 dB loss to $L_{\text{TX-ANT,ANT-INT}}$ due to the compression while computing the efficiency. To maintain fairness between the different antenna interfaces, we have evaluated $\eta_{\text{ANT-INT}}$ for different antenna interfaces while they operate with a PA with a nominal $\eta_{\text{PA}} = 30\%$ and $P_{\text{out,PA}}$ as the maximum TX power handling of the interface. In scenarios where DC power consumption of the power amplifier is only a small portion of the overall system power consumption, the degradation in overall system efficiency can be calculated by treating the antenna interface efficiency as the additional degradation in the PA efficiency (i.e., $\eta_{\text{PA,in FD}} = \eta_{\text{PA}} \times \eta_{\text{ANT}}$).

A few of the best integrated antenna interface implementations, in terms of the antenna interface efficiency shown in Table I, include the antenna interfaces reported in [53] (in 45 nm CMOS), [78] (in 65 nm CMOS) and [24] (in 180 nm CMOS) which have efficiencies of 54.7%, 31.6%, and 27.6%, respectively. In particular, [53] is a multi-feed antenna design which permits the TX and RX ports to be connected to different physical locations on the antenna such that the output from the TX port does not leak into the

RX. Due to the absence of any additional circuitry, the TX-ANT insertion loss and the ANT-RX noise figure are very low in this implementation while consuming no DC power thus providing a very high efficiency. However, the multi-feed antenna design fixes the antenna architecture which prevents it being operated with a commercial off-the-shelf antenna. The high efficiency of [78] is due to no added TX-ANT insertion loss and no DC power consumption with only the ANT-RX NF degrading the antenna interface efficiency. However, typical distributed PA architectures have reduced PA efficiency while the antenna interface efficiency can remain high. Ferrite circulators can have very high antenna interface efficiencies of 60–90% [90] due to their extremely low insertion losses. For example, [99] is a commercial off the shelf ferrite circulator having >83% efficiency. However, these circulators tend to be bulky and expensive devices that are currently not suitable for low-cost, small-form-factor applications. Hence, integrated circulators were proposed as an alternative. The first CMOS circulator reported in 2016 [38] has an efficiency of 4.4% due to its high power consumption and low isolation. However, in recent years the performance of these on-chip circulators has significantly improved. For instance, a recent CMOS circulator reported in [24] has an efficiency of 27.6%. While this still lags the ferrite circulators by a factor of 2, the performance gap is reducing, and further improving the integrated circulator efficiency by reducing its insertion losses is an important future research direction.

2) Isolation Fractional Bandwidth Product

The isolation fractional bandwidth product is simply the product of the isolation and the fractional bandwidth for which the isolation is obtained. Ideally we would like to define fractional bandwidth for a fixed target isolation level as a figure of merit of the antenna interface, however, since most works report different isolation levels, we choose to define the figure of merit as the product of isolation and fractional bandwidth:

$$\text{ISO-FBW} = ISO \times \frac{B}{f_c}, \tag{2}$$

where ISO-FBW is the isolation-FBW product for an antenna interface providing an isolation of ISO across a bandwidth of B at a center frequency of f_c.

Among the various antenna interface implementations, the EBD reported in [20] has the highest isolation bandwidth product (>39.9 dB) by leveraging a more complex RLC balancing network which provides up to 50 dB isolation across 200 MHz bandwidth (at 1.95 GHz center frequency). However, due to the high TX-ANT losses and ANT-RX noise figure, the antenna interface efficiency of EBDs has been low, which motivates integrated circulator implementations. Initial implementations of time modulated cirulators using N-path filters [29], [39] and angular momentum biasing [31] were inherently narrowband which resulted in a low isolation fractional bandwidth product. Recent implementations using switched transmission lines [25], [35] and switched bandpass filters [27] have provided wideband isolation and hence a higher isolation fractional bandwidth product. Most surveyed works have isolation fractional bandwidth product which are of the order of 10–30 dB which is comparable to that of ferrite circulators. Other works were also presented recently with extremely high isolation-fractional bandwidth products [26], [85].

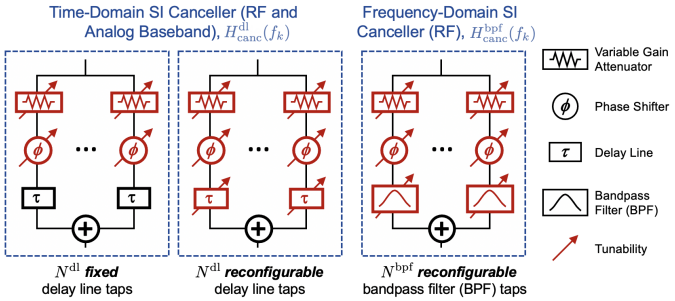

Fig. 4: Block diagrams of the time-domain and frequency-domain self-interference (SI) cancellers in RF and/or analog baseband (BB), with different tuning degrees of freedom (DoF).

Fig. 3(a) and 3(b) show the performance comparison of various integrated antenna interfaces in terms of the TX-RX isolation as a function of the isolation bandwidth and FBW (see also Table I). Fig. 3(c) shows the trade-offs between antenna interface efficiency and isolation bandwidth for the different surveyed works. From Fig. 3(c), it can be observed that both the antenna interface efficiency and the isolation-FBW product have been following an increasing trend over the years.

III. Two Types of Self-Interference Canceller

In this section, we describe two types of SI cancellers: (i) *time-domain* SI cancellers employing parallel delay line (DL) taps in *both* RF and analog baseband (BB) domains, and (ii) *frequency-domain* SI cancellers employing parallel bandpass filter (BPF) taps *only* in the RF domain. The block diagram of a time-/frequency-domain canceller with different tuning capabilities is shown in Fig. 4, and the detailed comparison between the two types of cancellers is summarized in Table II. Both types of SI cancellers with different settings have been demonstrated on ICs, as described in Sections IV and VII.

A. Notation

Consider a total wireless bandwidth of B that is divided into K orthogonal frequency channels indexed by $k = \{1, \ldots, K\}$ with the center frequency of the k^{th} channel denoted by f_k. We use discrete frequencies $\{f_k\}$ since in practical systems, the channel response is measured at discrete points (e.g., per OFDM subcarrier). However, the presented model can also be applied to cases with continuous frequency values. We denote the frequency response of the SI channel by $H_{\text{SI}}(f_k)$ with amplitude $|H_{\text{SI}}(f_k)|$ and phase $\angle H_{\text{SI}}(f_k)$. The transfer functions of a time-domain and frequency-domain SI canceller are denoted by $H_{\text{canc}}^{\text{dl}}(f_k)$ and $H_{\text{canc}}^{\text{bpf}}(f_k)$, respectively. An SI canceller has a number of *tunable parameters*, or *degrees of freedom (DoF)*, that need to be configured so that its frequency response, $H_{\text{canc}}^{\text{dl/bpf}}(f_k)$, closely matches with that of the SI channel, $H_{\text{SI}}(f_k)$. We would like to note that this model can also be applied for analog BB cancellers by considering frequencies $\{f_k\}$ in IF/BB.

TABLE II: Summary and comparison of two types of SI cancellers: *time-domain* SI cancellers employing parallel delay line (DL) taps in the RF/analog baseband, and *frequency-domain* SI cancellers employing parallel bandpass filter (BPF) taps in the RF domain.

Approach	Time-domain approach		Frequency-domain approach
SI Cancellation Domain	RF and/or analog baseband (BB)		RF
Canceller Transfer Function	$H_{\text{canc}}^{\text{dl}}(f_k) = \sum_{n=1}^{N^{\text{dl}}} w_n^{\text{dl}} \cdot e^{-j2\pi f_k \tau_n}$		$H_{\text{canc}}^{\text{bpf}}(f_k) = \sum_{n=1}^{N^{\text{bpf}}} w_n^{\text{bpf}} \cdot \left[1 - jQ_n\left(\frac{f_{\text{c},n}}{f_k} - \frac{f_k}{f_{\text{c},n}}\right)\right]^{-1}$
Features	N^{dl} *fixed* DL taps	N^{dl} *reconfigurable* DL taps	N^{bpf} *reconfigurable* BPF taps
Fixed Parameters for the n^{th} Tap	τ_n	N/A	N/A
Tunable Configuration Parameters (DoF) for the n^{th} Tap	$\lvert w_n^{\text{dl}}\rvert,\ \angle w_n^{\text{dl}}$	$\tau_n,\ \lvert w_n^{\text{dl}}\rvert,\ \angle w_n^{\text{dl}}$	$\lvert w_n^{\text{bpf}}\rvert,\ \angle w_n^{\text{bpf}},\ f_{\text{c},n},\ Q_n$
Total # of Tunable Parameters (DoF), M	$2 \cdot N^{\text{dl}}$	$3 \cdot N^{\text{dl}}$	$4 \cdot N^{\text{bpf}}$
Example Hardware Implementations	See Table III and Section VII		
Adaptive Tuning Algorithms	Minimum mean square error (MMSE): SI channel is required (e.g., [7], [41], [43], [46]) Dithered linear search (DLS): SI channel is not required (e.g., [42])		

B. Time-domain SI Cancellers

A time-domain SI canceller (in RF and/or analog BB) consisting of N^{dl} parallel DL taps has a transfer function given by

$$H_{\text{canc}}^{\text{dl}}(f_k) = \sum_{n=1}^{N^{\text{dl}}} w_n^{\text{dl}} \cdot e^{-j2\pi f_k \tau_n}, \tag{3}$$

where τ_n and w_n^{dl} represent the (real-valued) delay and (complex-valued) weight of the n^{th} DL tap, respectively. Essentially, multiple DL taps with different delays are combined to realized a finite impulse response (FIR) filter, which is used to better emulate the SI channel (i.e., performing *time-domain equalization*) to achieve wideband SIC in the RF and/or analog BB domains.

In particular, each canceller tap can be associated with a *fixed* or *reconfigurable* DL (see Fig. 4), which introduces delay to a signal. In the case with *fixed* DL taps, the delay values are usually selected based on the estimated delay spread of the SI channel and are fixed prior to the canceller fabrication. More importantly, the delay values are usually flat across the desired bandwidth. The time-domain canceller configuration vector, $\mathbf{c}^{\text{dl}} = [\mathbf{a}^{\text{dl}}, \phi^{\text{dl}}]$, includes the amplitude and phase of each tap, resulting in $2N^{\text{dl}}$ DoF. For example, an RF canceller with 16 DL taps and real-valued weights was presented in [7], where 8 taps are with delays of around 0.4 ns while the other 8 taps are with delays of around 1.4 ns. Another example is an RF canceller with 4 DL taps and complex-valued weights presented in [42], where the 4 taps are designed with delays of around 0/4/8/12 ns to cover an SI channel with significant delay spread. In the case with *reconfigurable* DL taps, the delay values τ can be tuned during operation, and the corresponding canceller configuration includes the delay, amplitude, and phase of each tap, resulting in $3N^{\text{dl}}$ DoF. For example, in [46], we designed and implemented a CMOS FD receiver integrating a 7-tap RF canceller and a 7-tap analog BB canceller, both of which have reconfigurable DL taps with a delay tuning range of 0.2–1.1/10–75 ns in the RF/analog BB domain using real-valued weights in the RF canceller and complex-valued weights in the BB canceller. In [44], we designed and implemented an improved version of the aforementioned CMOS FD receiver with a 16-tap RF canceller and an 8-tap analog BB canceller with a higher delay tuning rage of 0–7.75/0–85 ns in the RF/analog BB domain.

C. Frequency-domain RF Cancellers

A frequency-domain SI canceller (in RF) consisting of N^{bpf} parallel 2$^{\text{nd}}$-order BPF taps has a transfer function given by

$$H_{\text{canc}}^{\text{bpf}}(f_k) = \sum_{n=1}^{N^{\text{bpf}}} w_n^{\text{bpf}} \cdot \left[1 - jQ_n\left(\frac{f_{\text{c},n}}{f_k} - \frac{f_k}{f_{\text{c},n}}\right)\right]^{-1}, \tag{4}$$

where w_n^{bpf} represents the (complex-valued) weight applied to the n-th BPF tap with center frequency $f_{\text{c},n}$ (which is independent of f_k) and quality factor Q_n, respectively. Essentially, multiple BPF taps are used to emulate the SI channel (i.e., performing *frequency-domain equalization*, or *FDE*) to achieve wideband SIC in the RF domain. In this paper, we consider 2$^{\text{nd}}$-order BPF taps but this approach can also be extended to use any m^{th}-order ($m = 1, 2, \ldots$) RF filter taps.

In particular, each frequency-domain RF canceller tap is associated with a *reconfigurable* RF BPF (see Fig. 4), whose configuration includes the amplitude, phase, center frequency, and quality factor. As a result, each BPF tap features 4 DoF so that the SI channel can be emulated not only in amplitude and phase, but also in the slope of amplitude and the slope of phase (i.e., group delay). Therefore, unlike a DL tap that introduces delay to a signal using a *real delay line*, a BPF tap introduces delay to a signal using its tunable quality factor and its characteristics may vary across the cancellation bandwidth. In [66] and [43], we designed and implemented a frequency-domain RF canceller on an IC and a PCB, respectively, each consisting of 2 reconfigurable BPF taps with a total number of 8 tunable DoF.

D. Ideal Models vs. Practical Implementations

Ideal SI Canceller Models. The SI canceller models described in Sections III-B and III-C assume an *ideal* canceller transfer function given by (3) and (4), respectively (see also Table II). In particular, each tunable DoF has infinite resolution with no quantization constraints. In addition, there are no mutual effects between the RF canceller configuration parameters (e.g., changing the tap amplitude will not affect its phase response). Moreover, each DL tap in a time-domain canceller has frequency-flat amplitude response and linear phase response, and each BPF tap in a frequency-domain canceller has an ideal BPF response. For example, the 2$^{\text{nd}}$-order BPF in the n^{th} tap has a "bell shape" amplitude response with center frequency of $f_{\text{c},n}$ and 3 dB bandwidth of $f_{\text{c},n}/Q_n$.

Practical SI Canceller Implementations. In practice, an SI canceller hardware implementation (on an IC or a PCB) usually has a transfer function that deviates from the ideal model. For example, electromagnetic coupling will exist across the canceller taps and a DL tap may have frequency-selective amplitude response. Mutual coupling between the canceller configuration parameters will also introduce extra complexity when an adaptive tuning algorithm operates in an irregular configuration parameter space. Moreover, each tunable DoF is associated with certain tuning range and quantization (e.g., phase control with 8-bit resolution within the 360° tuning range [43]), which will affect and limit the performance of SIC in the RF and analog BB domains. In Section VI, we evaluate the effects of practical quantizations on the achievable SIC for representative canceller models.

IV. Integrated RF and Analog Baseband Self-Interference Cancellers

In this section, we provide a comprehensive overview and comparison of recent IC-based RF and analog baseband (BB) canceller implementations, whose details are summarized in Table III. In general, we consider two types of cancellers using the *time-domain* and *frequency-domain* approaches as described in Section III and Table II. For comprehensiveness, Table III also includes a third type: *amplitude and phase-based* cancellers, which are essentially time-domain cancellers with only one RF or analog BB tap.

A. Integrated RF SI Cancellers

In an FD radio, the residual SI after the TX-RX isolation provided by the antenna interface must be further suppressed in the RF and analog BB domains before the desired signal can be received with sufficient signal-to-noise ratio (SNR). Different types of SI cancellers have been implemented on ICs, which tap a portion of the TX signal and inject it into the RX to obtain cancellation. Injecting the tapped TX signal directly into the RX with a constant amplitude and phase scaling can emulate the frequency response of the SI channel only at a single frequency point, thus limiting the cancellation bandwidth. Amplitude- and phase-based cancellers have only a single delay present in the canceller and cannot cancel the large delays introduced by multi-path components, therefore limiting the amount of cancellation that can be obtained. The large delay spreads in the SI channel due to environmental effects and multiple coupling paths at the antenna interface require the cancellers to shape the TX signal in response to the SI channel before injecting it into the RX to perform wideband cancellation. To achieve this, these cancellers pass the coupled TX signal through re-configurable adaptive filters which closely emulate the SI channel. As described in Section III, these re-configurable filters can be designed as a bank of delay line (DL) elements to realize a finite impulse response (FIR) filter in the *time-domain*, or as a bank of bandpass filters (BPF) to emulate the SI channel in the *frequency-domain*. These cancellers with multiple taps can better emulate the multipath components, thus resulting in a higher cancellation bandwidth. Furthermore, most of the analog domain cancellers designed to operate at mmWave frequencies are amplitude and phase based as realizing true time delays at mmWave frequencies remains a challenge and is a subject of future research.

1) Integrated Time-Domain RF Cancellers

As described in Section III-B, time-domain cancellers tap a portion of the TX signal and pass it through multiple taps with different delays. The outputs of these parallel taps are then weighted (e.g., amplified/attenuated and phase shifted) and combined to realize an FIR filter in the RF domain. The weights corresponding to each tap need to be chosen such that the total frequency response of the FIR filter closely matches that of the SI channel. The output of the FIR filter is then injected into the RX and RF SIC is performed at the RX input.

Various techniques to realize integrated time-domain RF cancellers through different implementations of true-time delays in ICs have been proposed [15], [16], [28], [44], [46], [57]. Transmission lines are the most basic elements which provide true-time delays across a wide bandwidth. As described in Section VI, nanosecond-scale delays are required to achieve sufficient amount of RF SIC across wide bandwidth for a given antenna interface. However, realizing transmission lines with nanosecond-scale delays, especially for implementations with multiple delay taps, requires prohibitively large area that is unsuitable for compact IC designs. For example, obtaining a nanosecond delay in silicon typically requires a 15 cm-long delay line.

One technique to realize an approximation of true time delays on ICs is using first-order RC-CR all pass filters (APFs) [16], [56], [57]. The delay elements in these passive RF canceller implementations do not consume any DC power and have high linearity as well as compact form-factor due to the absence of inductors. However, these filters produce delays that are inversely proportional to the operating frequency and therefore it is challenging to achieve large delays at operating frequencies of the order of 1 GHz. For example, in [56], [57], RC-CR filters achieving nominal delays of up to 65 ps have been realized. By cascading 5 such delay elements and tapping from the output of each delay element, a 5-tap FIR filter achieving a total delay of up to 250–300 ps has been implemented. Along with additional SIC in the analog BB domain, this canceller achieves 50 dB cancellation across 42 MHz at 1.9 GHz operating frequency with a 50 Ω termination at the

TABLE III: Summary and comparison of IC-based RF/analog baseband (BB) canceller implementations.

Work	Category	Operating Frequency	# of Taps (domain)	DoF per Tap	SIC/ Bandwidth @Frequency	Canceller Power Consumption	Rx NF (NF degradation with canceller)	SI Power Handling	Technology/ Area	Canceller Efficiency	SIC-FBW Product
ISSCC'21 [44]	Time-domain	0.1–1.0 GHz	16 (RF) + 8 (BB)	1 (RF), 4 (BB)	42 dB/40 MHz @800 MHz	44.8 mW (RF and BB)	3.7 dB (0.8 dB)	−12 dBm	65 nm/ 7.2 mm^2	43.5%	29.0 dB
ISSCC'20 [45]	Amp. & Phase-based	28/37 GHz	1/4 for SISO/2×2 MIMO (RF)	2 (RF)	25 dB/100 MHz @28 GHz	N/A (Rx total: 98.75 mW)	7.9 dB (N/A)	N/A	65 nm/ 1.05 mm^2	N/C	0.5 dB
RFIC'20 [46]	Time-domain	0.1–1.0 GHz	7 (RF) + 7 (BB)	1 (RF), 4 (BB)	30 dB/20 MHz @738 MHz	32 mW (RF and BB)	5.3 dB (1.9 dB)	−13 dBm	65 nm/ 5.15 mm^2	31.4%	14.3 dB
IMS'20 [15]	Time-domain	1.5–2.0 GHz	2 (RF) + 2 (BB)	2 (RF), 2 (BB)	28 dB/100 MHz @1.7 GHz	45 mW	4.9 dB (1.3 dB)	−20 dBm	65 nm/ 1.5 mm^2	11.1%	15.7 dB
ISSCC'19 [28], JSSC'19 [29]	Time-domain	2.2 GHz	4/16 for SISO/2×2 MIMO (BB)	1 (BB)	SIC: 30 dB/20 MHz, 2×2 CT-SIC: 23 dB/20 MHz @2.2 GHz	25 mW, per element	11.2 dB (1.7 dB)	−1 dBm	65 nm/ 2.8 mm^2, per element	21.0%	9.6 dB
ISSCC'19 [47], JSSC'20 [48]	Amp. & Phase-based	28/37/39 GHz	1 (RF)	2 (RF)	26 dB/500 MHz @28 GHz	N/A (Rx total: 37.6 mW)	6.2 dB (N/A)	N/A	65 nm/ 0.48 mm^2	N/C	18.5 dB
RFIC'19 [49], JSSC'20 [50]	Amp. & Phase-based	0.5–2.5 GHz	1/4 for SISO/2×2 MIMO (BB)	2 (BB)	SIC: 29 dB/20 MHz, 2×2 CT-SIC: 24 dB/20 MHz @900 MHz	16–62 mW, per element	3.1 dB (1.3 dB)	−5 dBm	65 nm/ 3 mm^2	60.3%	12.5 dB
RFIC'19 [51], TMTT'20 [52]	Amp. & Phase-based	0.5–3.5 GHz	1 (RF)	2 (RF)	35 dB/10 MHz @2 GHz	4–12 mW	3.3 dB (2 dB)	−25 dBm	65 nm/ 1.5 mm^2	16.3%	12.0 dB
ISSCC'18 [53], JSSC'18 [54]	Amp. & Phase-based	60–75 GHz	1 (RF)	2 (RF)	25 dB/2 GHz @65 GHz	0 mW, passive	4.8 dB (<0.1 dB)	−24.5 dBm	45 nm/ 7.3 mm^2	86.9%	9.9 dB
ISSCC'18 [16], CICC'18 [55]	Time-domain	1.6–1.9 GHz	10 (RF)	1 (RF)	31 dB/40 MHz @1.77 GHz	14.3 mW	2.5 dB (1.6 dB)	N/A	40 nm/ 4.0 mm^2	N/C	14.6 dB
ISSCC'17 [56], JSSC'18 [57]	Time-domain	1.7–2.2 GHz	5 (RF) + 14 (BB)	1 (RF), 1 (BB)	50 dB/42 MHz @1.9 GHz	3.5 mW (RF), 8 mW (BB)	4 dB (1.55 dB)	−13 dBm	40 nm/ 3.5 mm^2	48.0%	33.4 dB
RFIC'17 [58], TCAS-I'18 [59]	Time-domain	0.9 GHz	2 (RF)	2 (RF)	23 dB/80 MHz @900 MHz	13 mW	9.6 dB (1.4 dB)	N/A	130 nm/ 0.72 mm^2	N/C	12.5 dB
RFIC'17 [60], JSSC'18 [61]	Amp. & Phase-based	1–3 GHz	1 (RF)	2 (RF)	20 dB/15 MHz @2.3 GHz	0 mW, passive	4 dB (0.4 dB)	−5 dBm	28 nm/ 0.5 mm^2	71.7%	−1.9 dB
ESSCIRC'17 [62]	Amp. & Phase-based	1–3 GHz	1 (RF)	2 (RF)	30 dB/4 MHz @2.4 GHz	0.25 mW	4.3 dB (0.6 dB)	−20 dBm	40 nm/ 1.95 mm^2	73.3%	2.2 dB
ISSCC'16 [38], JSSC'17 [39]	Amp. & Phase-based	0.6–0.8 GHz	1 (BB)	2 (BB)	22 dB/12 MHz @750 MHz	30 mW	5.0 dB (1.6 dB)	−24 dBm	40 nm/ 1.4 mm^2	6.5%	4.0 dB
IMS'16 [63], JSSC'16 [64]	Amp. & Phase-based	3.8–4.8 GHz	1 (RF)	2 (RF)	32–36 dB/N/A @4.3 GHz	N/A (transceiver total: 2 W)	3.1 dB (0.6 dB)	N/A	130 nm SiGe BiCMOS/ 12 mm^2	N/C	N/C
ISSCC'15 [65], JSSC'15 [66]	Freq.-domain	0.8–1.4 GHz	2 (RF)	4 (RF)	20 dB/25 MHz @1.37 GHz	44–91 mW, per tap	4.8 dB (1.3 dB)	−8 dBm	65 nm/ 4.0 mm^2	32.5%	2.6 dB
ISSCC'15 [67], JSSC'15 [68]	Amp. & Phase-based	0.2–3.5 GHz	1 (RF)	2 (RF)	27 dB/16 MHz @2.5 GHz	10 mW	6.3 dB (4 dB)	−16.4 dBm	65 nm/ 2 mm^2	15%	5.1 dB
RFIC'15 [69], JSSC'16 [70]	Amp. & Phase-based	60 GHz	1 (RF)	2 (RF)	20 dB/1 GHz @59 GHz	44 mW	4 dB (<0.1 dB)	N/A	40 nm/ 4.42 mm^2	N/C	2.3 dB

(i) DoF: Degree of Freedom; NF: Noise Figure; SIC-FBW Product: SIC-Fractional Bandwidth (FBW) Product (see (6) in Section IV-C).
(ii) N/A: Not Available/Applicable, i.e., metric was not reported in the specific implementation. N/C: Not Computable.

antenna port. In [16], similar RC-CR APFs are used to realize a delay of 50.9 ps. Two 5-tap filters were implemented using these delay cells with the first filter injecting the cancellation current at the LNA input and the second filter injecting the cancellation current at the LNA output. This effectively realizes a 10-tap FIR filter, which achieves 31 dB SIC across 40 MHz bandwidth at 1.77 GHz with 50 Ω termination at the antenna port.

Another technique to realize large true time delays with small form factors is based on the sample-hold-and-release principle in switched-capacitor circuits. In such approaches, the input signal is periodically sampled onto a capacitor and the stored sample is sensed at the output through a switch controlled by a delayed version of the sampling clock. The delay between the input and output clocks imparts a true time delay to the input signal. The bandwidth of this circuit is proportional to the clocking frequency and the maximum delay imparted is proportional to clocking period, thereby creating a trade-off between the bandwidth and maximum delay imparted. This trade-off can be surpassed by using non-overlapping layers of these switched capacitor structures. Essentially having N parallel non-overlapping layers enhances the delay-bandwidth product by N times, which can used to leverage delay elements with N times larger bandwidth which achieves the same delay or vice versa.

In [46], these N-path switched-capacitor circuits were implemented to achieve up to 1.1 ns delay in the RF domain, and a 7-tap FIR filter is realized using 7 such delay elements in parallel. Summation of the tap outputs is achieved passively through charge sharing between the sampling capacitors which is then injected into the RX input in the current domain. Using this prototype, 13 dB RF SIC has been achieved across 20 MHz bandwidth at 738 MHz operating frequency with a circulator-based antenna interface terminated with a commercial off-the-shelf antenna. In [44], a similar switched-capacitor-based delay has been implemented with capacitive-stacking to obtain passive voltage gain which compensates the loss introduced by the switched-capacitor circuits and improves the canceller noise and power handling performance. As mentioned earlier, interleaving a higher number of single path switched-capacitor layers enables higher delays. It was shown that delays up to 7.75 ns can be achieved using 32-path switched capacitor delays clocked at 500MHz, which were used to realize a 16-tap FIR filter with programmable delays. The LNTA in the RX has been modified to absorb the operations of FIR weighting, summation, and injection, which removes the need of additional injection circuitry and thus improves the noise performance of the integrated FD receiver. This prototype achieves 30 dB cancellation across 40 MHz bandwidth at 800 MHz operating frequency with a circulator whose antenna port is terminated with 50 Ω impedance.

A third technique to obtain RF delays is to downconvert the RF signal into baseband, obtain the delay in baseband, and then up-convert the delayed signal back to the RF domain. One advantage of this technique is the availability of I/Q paths in the baseband if IQ-downconversion is applied, thus enabling complex-valued weighting of the RF canceller taps. This technique has been implemented in [58] by utilizing the delay of an RC low pass filter to implement baseband delays. A 2-tap FIR filter was implemented using these delays, which achieves 23 dB SIC across 80 MHz bandwidth at 900 MHz operating frequency. A similar approach utilizing delays generated in baseband to perform RF SIC was presented in [15]. In particular, the FD receiver is implemented with a passive mixer-first architecture and the tapped TX signal is down-converted to BB frequencies and passed through an N-path delay. Then, the BB cancellation signal is injected into the receiver after the passive mixer. Due to the bi-directional transparency of the passive mixer, the cancellation signal is up-converted back to RF at the RX input to perform RF SIC. Together with a separate explicit analog BB canceller, this implementation achieves a total RF SIC of 28 dB across 100 MHz at 2.7 GHz operating frequency.

2) Integrated Frequency-Domain RF Cancellers

As described in Section III-C, SI cancellers employing the frequency-domain approach tap a portion of the TX signal and pass it through a bank of reconfigurable RF BPFs (see Fig. 4). The outputs of these parallel BPFs are then combined and RF SIC is performed at the RX input. In particular, each BPF tap features 4 DoF including the amplitude, phase, center frequency, and quality factor, which can be tuned such that the combined frequency responses of multiple BPFs matches that of the SI channel across wide bandwidth.

To implement the desired RF BPFs, second-order G_m–C-based N-path filters were proposed in [65], which have emerged as a promising solution to obtain reconfigurable BPFs with high quality factors. The quality factor and phase of a two port N-path filter can be easily controlled by varying the path capacitance and the delay between the two sets of switches, respectively. By using clockwise/counter-clockwise connected transconductors between the paths of an N-path filter, an upward/downward frequency offset with respect to the switching frequency can be obtained, which allows for tuning the center frequency of the filter by varying the trans-conductance. N-path filter-based implementation of BPFs consume smaller chip area than LC-based implementations due to the absence of inductors and therefore can be easily implemented in CMOS. However, the presence of active transconductors for obtaining frequency tunability increases the power consumption and noise produced in such implementations. The frequency-domain RF canceller featuring two BPF taps presented in [65] achieves 20 dB RF SIC across 25 MHz bandwidth at 1.37 GHz operating frequency (with 30 dB initial isolation achieved by an antenna pair) and has a DC power consumption of ∼90–180 mW.

3) Other Integrated RF Cancellers

Apart from time-domain, frequency-domain, and amplitude and phase-based cancellers, other types of self-interference cancellers include code-domain cancellers and DAC based cancellers. Code-domain cancellers such as the ones reported in [100], [101] spread the TX signal by a PN code. The desired received signal is spread with a different PN code that is orthogonal to that of the TX signal's PN code. A code-domain RF correlator with high input power handling is used at the RX which unspreads the desired received signal with the RX signal's PN code while spreading the TX-SI out-of-band (OOB) due to the orthogonality between the TX and RX codes. DAC based SI cancellers [102] take the input from the digital TX data directly and injects into the input of the LNA to provide cancellation. However, such implementations cannot cancel the noise and nonlinear components of the actual radiated TX signal. The DAC based SI canceller in [102] provides 64 dB cancellation across 20 MHz bandwidth.

B. Integrated Analog Baseband Cancellers

Time-domain analog BB cancellers are implemented by realizing delays using similar methods as those used in the time-domain RF cancellers. However, due to the lower bandwidth requirement for the delays in the analog BB, larger delays can be easily achieved, which allows for further improved SIC performance by emulating the weaker TX-RX coupling paths that usually have larger delays.

Techniques to obtain delays in the analog BB include the use of G_m–C-based APFs, which consume much smaller chip areas compared to using RC-CR APFs. These filters have been shown to provide a delay of up to 10 ns [56], [57]. In particular, 13 such filters were cascaded to obtain a total delay spread of up to 130 ns, and the outputs of each of these delay cells are combined to realize a 14-tap FIR filter (including the tap with zero delay). In [28], similar cascaded active G_m–C APFs were used to realize a 4-tap FIR filter for each TX-RX pair in a 2×2 MIMO transceiver, which achieved up to 120 ns delay for wideband SIC. This analog BB canceller provides 30 dB SIC across 20 MHz and 23 dB cross-talk SIC across 20 MHz.

Another technique to achieve large delays in the analog BB is through the use of multi-path switched-capacitor circuits based on the sample-hold-and-release principle, where the clocking frequency of the switched-capacitor circuits can be reduced due to the low bandwidth requirement of the baseband signals and achieve large delays at baseband. Using this technique, the analog BB canceller presented in [46] realizes a delay of up to 75 ns, and by using a 7-tap FIR filter, 17 dB SIC is achieved across 20 MHz bandwidth. An improved analog BB canceller using a similar approach was presented in [44], which realizes a delay of up to 85 ns, and by using an 8-tap FIR filter, 12 dB SIC is achieved across 40 MHz bandwidth.

C. Comparison and Figure of Merit (FOM)

Table III summarizes the comparison between different state-of-the-art RF and analog/BB cancellers. An ideal canceller needs to provide a sufficient amount of SIC across the desired bandwidth at a given center frequency, and handle a high SI power level while introducing low NF degradation of the RX. However, these metrics tradeoff with each other in realistic IC implementations. To provide a comprehensive and fair comparison, similar to the FOM defined for the antenna interfaces in Section II-D, we define two FOM for the cancellers: (i) the *canceller efficiency*, denoted by η_{Canc}, which taks into account the canceller's SI power handling and DC power consumption, the additional TX-ANT loss due to coupling power from the TX output, and the RX NF degradation, and (ii) the *SIC-fractional bandwidth (FBW) product*.

1) Canceller Efficiency

We consider an FD radio consisting of the same PA described in Section II-D1, and a canceller with an added TX-ANT loss of $L_{\text{TX-ANT,Canc}}$, NF degradation of NF_{Canc}, and DC power consumption of $P_{\text{DC,Canc}}$. Similar to (1), the canceller efficiency, η_{Canc}, is given by

$$\eta_{\text{CANC}} = \frac{P_{\text{out,PA}} \times L_{\text{TX-ANT,Canc}}/NF_{\text{Canc}}}{P_{\text{out,PA}}/\eta_{\text{PA}} + P_{\text{DC,Canc}}} \times \frac{1}{\eta_{\text{PA}}} \times 100\% \quad (5)$$

Additionally, in scenarios where the DC power consumption of the power amplifier is only a small portion of the overall system power consumption, the degradation in overall system efficiency can be calculated by treating the canceller efficiency as the additional degradation in the PA efficiency (i.e., $\eta_{\text{PA,in FD}} = \eta_{\text{PA}} \times \eta_{\text{Canc}}$).

In an FD system, the PA output power, $P_{\text{out,PA}}$, is limited by the maximum SI power handling of the canceller for a given initial isolation achieved by the antenna interface. The total gain of the SI canceller from the TX output to the RX input consists of three main components: (i) the TX coupling factor, C_{TX}, (ii) the gain of the canceller with filter taps, G_{Canc}, and (iii) the RX coupling factor, C_{RX}. The total gain of the canceller, given by $C_{\text{TX}} \cdot G_{\text{Canc}} \cdot C_{\text{RX}}$, must be equal to the initial antenna interface isolation in magnitude to achieve high SIC from the canceller. A higher initial isolation will allow for coupling less power either from the TX or into the RX to perform cancellation. Coupling less power from the TX reduces the voltage swing at the input of the canceller and therefore, increases the SI power handling. Coupling less power into the RX reduces the amount of noise added by the canceller and therefore, reduces the NF degradation of the RX due to the additional canceller circuitry.

Since a canceller always operates in conjunction with an antenna interface, to maintain fairness in comparison across different implementations, we evaluate the canceller efficiency assuming the same initial isolation of 25 dB, and a PA efficiency of $\eta_{\text{PA}} = 30\%$. $P_{\text{out,PA}}$ is taken to be $P_{\text{SI,max,Canc}} \times 10^{25/10}$ where $P_{\text{SI,max,Canc}}$ is the maximum SI power handling of the canceller. We then normalize the NF degradation of different cancellers by re-evaluating the NF degradation when the canceller operates in conjunction with an RX with 3 dB NF. We would like to note that the TX-ANT loss due to the canceller circuitry is not reported in many instances in prior works reviewed in Table III. In such cases, we assume a -10 dB coupling factor as the nominal coupling from the TX to the canceller, based on which the TX-ANT loss due to this coupling can be computed. In addition, for a canceller to operate in the linear regime, the amount of residual SI must be lower than the maximum SI power handling capability of the canceller. Hence, for a given amount of TX power, it is desired that the TX-RX isolation achieved by the antenna interface satisfies $ISO \geq P_{\text{TX}} - P_{\text{SI,max,Canc}}$ where P_{TX} is the TX power and $P_{\text{SI,max,Canc}}$ is the maximum SI power handling of the canceller.

The best integrated canceller implementations, in terms of antenna interface efficiency shown in Table III, include [53] (in 45 nm CMOS), [60] (in 28 nm CMOS), and [62] (in 40 nm CMOS), all of which are amplitude and phase-based cancellers and have a canceller efficiency of >70%. Such a high efficiency is attributed to their low power consumption where [53] and [60] use completely passive implementations, while the canceller reported in [62] has a DC power consumption of only 0.25 mW. In addition, the NF degradation introduced by these implementations is very low. However, due to the absence of multiple time-domain or frequency-domain filter taps, these implementations have lower SIC-FBW products. Moreover, completely passive implementations of time- or frequency-

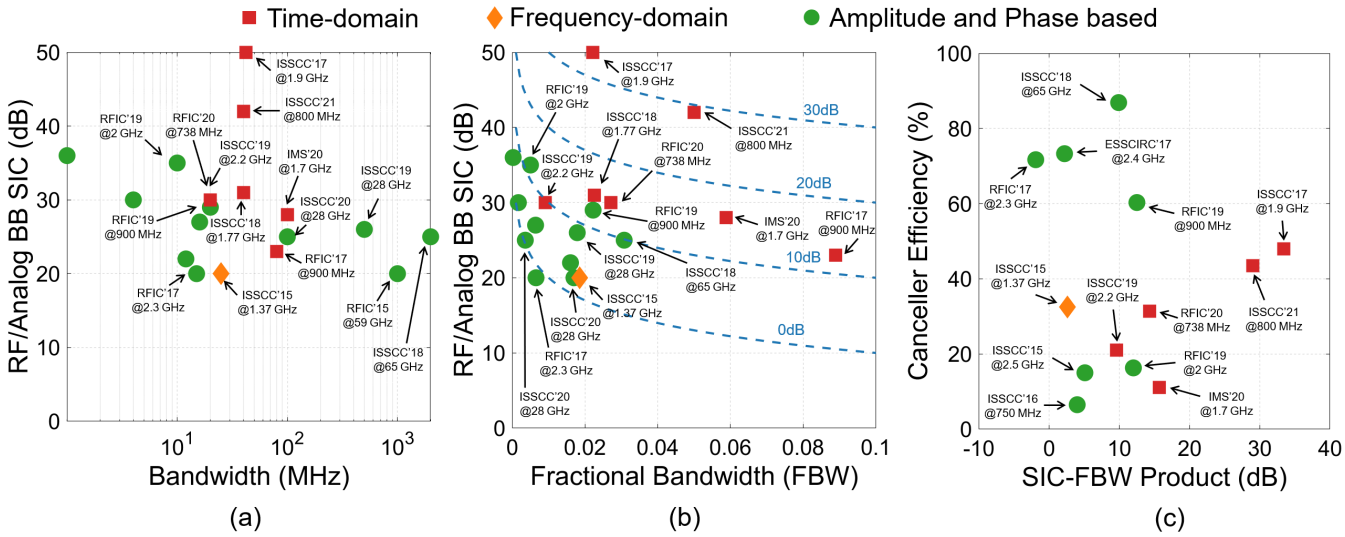

Fig. 5: Self-interference cancellation (SIC) achieved by various integrated cancellers in RF and/or analog BB domains as a function of the (a) SIC bandwidth and (b) fractional bandwidth (with contours indicating constant SIC fractional bandwidth product). (c) Canceller efficiency achieved by various integrated cancellers as a function of the SIC fractional bandwidth product.

domain cancellers using CMOS technologies will consume a large area and, to the best of our knowledge, have not been demonstrated on ICs.

Among the time- and frequency-domain canceller implementations that achieve the best SIC performance, [56] and [44], which are both time-domain cancellers, have a canceller efficiency of 48% and 43.5%, respectively. The frequency-domain canceller reported in [65] has an efficiency of 32.5% when two BPF filter taps are used. In particular, the canceller in [56] has a low power consumption which is responsible for its high efficiency. The NF degradation in [44] is very minimal and has a moderate power consumption thereby leading to a high canceller efficiency. The frequency-domain canceller in [65] has a higher power consumption level compared with the two aforementioned time-domain cancellers due to the presence of active transconductors in the BPF implementation, therefore degrading its efficiency.

2) Cancellation Fractional Bandwidth Product

Similar to (2), the SIC-FBW product of a canceller is defined as the product of the achieved amount of SIC, denoted by by SIC, and the FBW, B/f_c, i.e.,

$$\text{SIC-FBW} = SIC \times \frac{B}{f_c}. \tag{6}$$

Figs. 5(a) and 5(b) show the performance comparison of various integrated cancellers in terms of the achieved RF/analog BB SIC as a function of the bandwidth and FBW (see also Table III), and Fig. 5(c) shows the tradeoffs between the canceller efficiency and SIC-FBW product. Among the canceller implementations summarized in Table III, [56] and [44], which employ SIC in both RF and BB, achieve the highest SIC-FBW product. In particular, [56] is a time-domain canceller with 5 RF canceller taps (producing a delay of up to 250–300 ps) and 14 analog BB canceller taps (producing a total delay of 130 ns) which provides 50 dB cancellation across 42 MHz bandwidth (at 1.9 GHz center frequency) with a corresponding SIC-FBW product of 33.4 dB. The time-domain canceller reported in [44] uses switched-capacitor-based delays to realize the delay lines (unlike in [56] where RC-CR all-pass filters were used in RF and G_m–C APFs were used in the analog BB). These switched-capacitor-based delays can impart a higher delay in the RF domain compared to the RC-CR APF based delays for the same form factor. The amount of delay produced by these switched capacitor delays is similar to the total delay produced by cascaded G_m–C APFs at baseband frequencies. This canceller has 16 RF taps producing delay up to 8 ns and 8 BB taps producing delay up to 85 ns, which provides 42 dB cancellation across 40 MHz bandwidth (at 800 MHz center frequency) with a corresponding SIC-FBW product of 29 dB.

In general, it can be observed that cancellers with multiple filter taps perform better than single tap amplitude and phase-based cancellers. Increasing the number of canceller taps usually increases the canceller's power consumption, noise figure (NF), and area. For example, in Gm–C APF delay based time-domain cancellers, a higher transconductance is required to obtain taps with higher delay values. Increasing the number of taps in any passive based approach would result in a higher area since the delay obtained is proportional to the area consumed. In switched-capacitor-based delays as well, the area and power consumption increases with a larger number of taps. However, the area used for switched capacitor delays is several orders of magnitude lower than for passive delays [46] and when clocking circuits are shared between the taps, the power consumption does not increase proportionally to the number of taps, leading to improved efficiency when a larger number of taps are implemented. Hence, the penalty from increasing the number of cancellation taps is very implementation-specific and tradeoffs should be evaluated with the SI canceller architecture in mind.

V. Adaptive Canceller Tuning Algorithms

To achieve optimized SIC performance in response to environmental changes, the SI canceller needs to be adaptively tuned in an efficient manner. In this section, we discuss two adaptive canceller tuning algorithms that can be applied to both the time-domain and frequency-domain cancellers (see Table II). The first algorithm is based on a *minimum mean square error (MMSE)* problem, where the canceller is configured to have a frequency response that is the most similar to $H_{\text{SI}}(f_k)$. The second algorithm is based on *dithered linear search (DLS)* from adaptive filter design, where the SI canceller is tuned based on only the RX signal strength and requires little information about the SI channel or the internal canceller state. While practical demonstrations of adaptive RF canceller tuning algorithms have been implemented using a host computer/laptop or an FPGA (e.g., see [7], [41]–[43]), their performance in terms of power and area consumption can be further improved using an application-specific integrated circuit (ASIC) implementation. In Section VI-D, we present case studies and numerical evaluations of both algorithms.

A. Minimum Mean Square Error (MMSE)

The MMSE-based algorithm is the most commonly applied method and has been implemented for both time-domain and frequency-domain cancellers [7], [41], [43], [46]. Essentially, based on the (real-time) SI channel measurements and canceller model, the MMSE-based algorithm solves for the canceller configuration so that the canceller response best matches (in mean square error) the SI channel across the desired bandwidth. This optimization problem can be formulated as

$$\min: \sum_{k=1}^{K} \left| H_{\text{SI}}(f_k) - H_{\text{canc}}^{\text{dl/bpf}}(f_k) \right|^2, \tag{7}$$

where the variables are the RF canceller configuration parameters described in Table II.

For a time-domain canceller with independent and frequency-flat amplitude and phase responses of each *fixed* DL tap, it was shown in [103] that the global optimal canceller weights can be obtained in closed-form by adopting analysis from the design of complex Wiener filters. In practice, it is challenging to obtain the global optimal weights, since the canceller configuration surface is usually non-convex due to implementation imperfections and mutual coupling between hardware components. For example, an iterative gradient descent algorithm applied to a time-domain RF canceller can achieve a sufficient amount of RF SIC with a locally optimal configuration and a fine-grained local search. Using such a method, the adaptive configuration of a time-domain canceller with 16 fixed RF DL taps and a total number of 16 configuration parameters [7] is finished within 1 ms using an FPGA implementation.

The MMSE-based algorithm can also be applied to a frequency-domain canceller with reconfigurable RF BPF taps. However, due to additional configuration parameters that appear in the denominator of $H_{\text{canc}}^{\text{bpf}}(f_k)$ (see Table II), only locally optimal configurations can be obtained even in the ideal case using a non-convex solver. For example, the adaptive configuration of a frequency-domain canceller with 2 programmable BPF taps and a total number of 8 configuration parameters [43] is finished within 10 ms on a regular PC. This performance can be significantly improved using an FPGA implementation.

B. Dithered Linear Search (DLS)

The dithered linear search (DLS) algorithm is an efficient gradient descent-based algorithm for analog filter adaptation. The key advantages of DLS are: (i) it can perform optimization over irregular (e.g., non-convex) state space, and (ii) it requires little information about the SI channel, $H_{\text{SI}}(f_k)$, and the internal canceller state, $H_{\text{canc}}^{\text{dl/bpf}}(f_k)$. The DLS algorithm was applied to a time-domain canceller implementation with 4 fixed RF DL taps with a total number of 8 configuration parameters [42], where the adaptive configuration is finished in about 0.5 ms. It can also be applied to other time- and frequency-domain cancellers.

The DLS algorithm operates in an iterative manner. We use $\mathbf{c}_{(\kappa)}$ to denote the canceller configuration in the κ^{th} iteration, which is a vector with dimension equal to its number of DoF, and use $P_{\text{res}}(\kappa)$ to denote the residual SI power after SIC in the κ^{th} iteration. With the measured residual SI power, the canceller configuration in the κ^{th} iteration is perturbed by a *dither signal*, denoted by $\mathbf{d}_{(\kappa)}$, which is uniformly distributed with zero mean, i.e., $\widetilde{\mathbf{c}}_{(\kappa+1)} = \mathbf{c}_{(\kappa)} + \mathbf{d}_{(\kappa)}$ (with $\mathbf{c} = \mathbf{c}^{\text{dl}}$ or $\mathbf{c}^{\text{bpf}}$). Then, the canceller configuration in the $(\kappa+1)^{\text{th}}$ iteration is updated based on

$$\mathbf{c}_{(\kappa+1)} = \mathbf{c}_{(\kappa)} - \mu \cdot [P_{\text{res}}(\kappa+1) - P_{\text{res}}(\kappa)] \cdot \mathbf{d}_{(\kappa)}, \tag{8}$$

where μ is a step size that controls the tradeoffs between the granularity and speed of convergence. It can be seen that the DLS algorithm requires only the information about the RX signal strength, $P_{\text{res}}(\kappa)$, which depends on both the SI channel and canceller model.

VI. Measurement-based Numerical Evaluations

In this section, we first describe the SI channel measurements and simulation setup. Then, we numerically evaluate the RF SIC performance of the time- and frequency-domain RF cancellers (excluding the TX-RX isolation provided by the antenna interface), and discuss various design tradeoffs. Note that although we focus on RF SIC achieved with the measured SI channel, $H_{\text{SI}}(f_k)$, in the RF domain, the same evaluations can also be extended to SIC in the analog BB domain using the time-domain approach.

A. SI Channel Measurements and Setup

SI Channel Measurements: To evaluate and compare the performance of RF cancellers with different SI channels, we consider both a shared antenna interface (an antenna with a coaxial circulator) and a separate antenna interface at different carrier frequencies. Specifically, we measure $H_{\text{SI}}(f_k)$ (i.e., frequency response of the SI channel) of the following three antenna interfaces using a vector network analyzer (VNA) and S-parameters measurements:

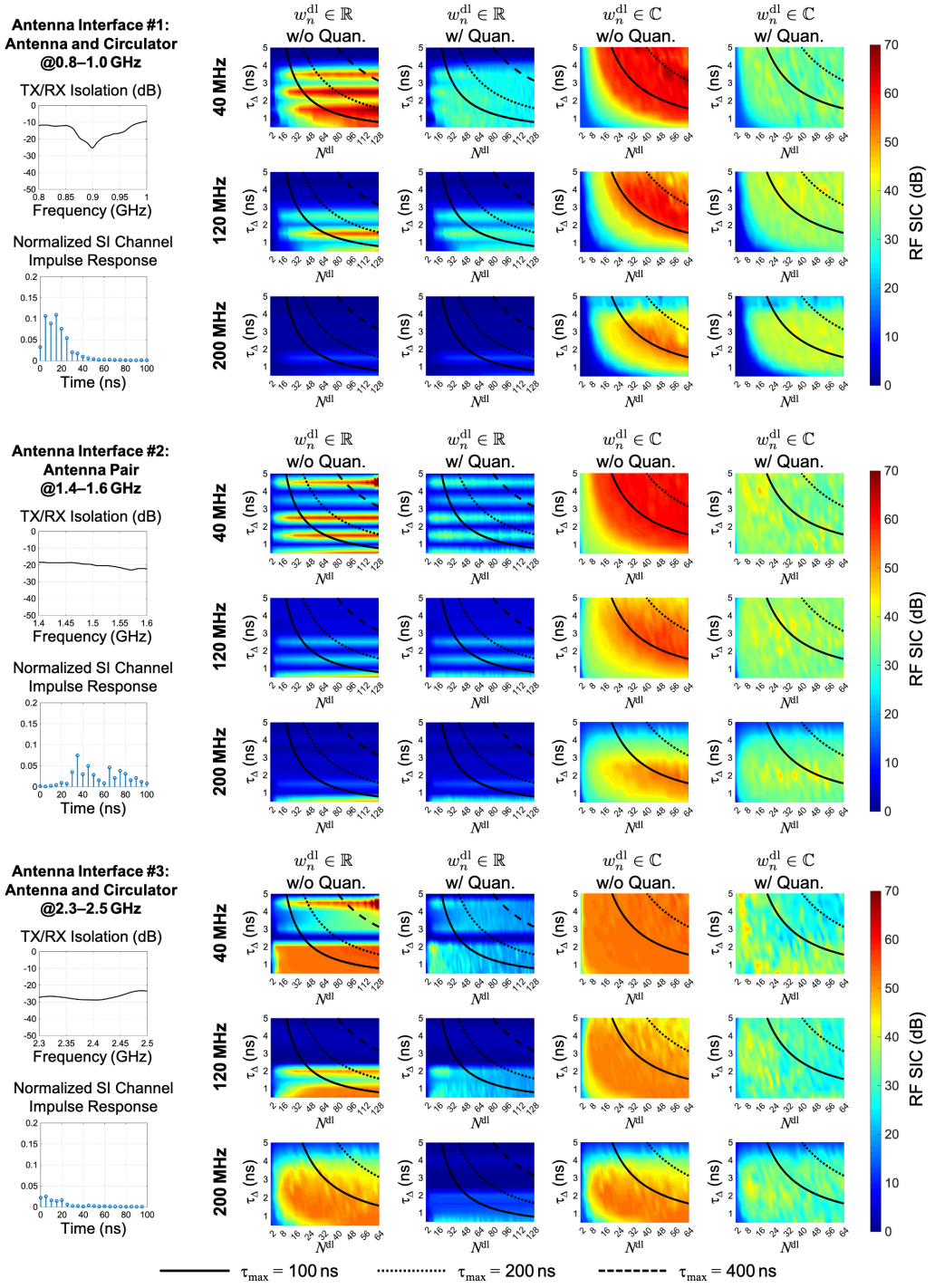

Fig. 6: Numerical evaluations of the achievable RF SIC using the time-domain approach employing *fixed* delay line (DL) taps (**Canc-DL-C** and **Canc-DL-R**), with varying number of DL taps (N^{dl}), DL step size (τ_Δ), three antenna interfaces (**Ant 1**, **Ant 2**, and **Ant 3**) at different frequencies, RF SIC bandwidth (B), in both the *ideal* (without quantizations) or *practical* (with quantizations) case.

- Antenna Interface 1 (**Ant 1**): An antenna with an RF-CI RFCR3204 coaxial circulator [104] at 0.8–1.0 GHz (a shared antenna interface at 0.9 GHz carrier frequency);
- Antenna Interface 2 (**Ant 2**): An antenna pair at 1.4–1.6 GHz (a separate antenna interface at 1.5 GHz carrier frequency);
- Antenna Interface 3 (**Ant 3**): An antenna with an RF-CI RFCR3810 coaxial circulator [99] at 2.3–2.5 GHz (a shared antenna interface at 2.4 GHz carrier frequency).

The SI channel characteristics, including the TX/RX isolation and impulse response, are shown in Fig. 6. Based on the measurements, we consider varying signal bandwidth of $B \in \{40, 120, 200\}$ MHz.

RF Canceller Setup: We consider time- and frequency-domain RF cancellers with varying number of DL and BPF taps and canceller settings. In this paper, we focus on the following three types of RF cancellers, which have all been

realized in practical systems (see Table II):

- **Canc-DL-R**: A time-domain RF canceller with N^{dl} *fixed* DL taps and real-valued weights, ($w_n^{\text{dl}} \in \mathbb{R}$, 1 DoF per DL tap);
- **Canc-DL-C**: A time-domain RF canceller with N^{dl} *fixed* DL taps and complex-valued weights ($w_n^{\text{dl}} \in \mathbb{C}$, 2 DoF per DL tap);
- **Canc-BPF**: A frequency-domain RF canceller with N^{bpf} *reconfigurable* BPF taps and complex-valued weights ($w_n^{\text{bpf}} \in \mathbb{C}$, 4 DoF per BPF tap).

To better understand the achievable RF SIC performance, *we apply an equal total number of DoF, denoted by M, to each type of RF canceller*. For example, $M = 128$ corresponds to 128 taps for Canc-DL-R, 64 taps for Canc-DL-C, and 32 taps for Canc-BPF (see Table II).[1] In this section, we focus on the achievable RF SIC assuming that the considered cancellers operate in their linear regime.

In the *ideal case without quantizations*, for each RF canceller tap, we set the amplitude and phase tuning range of $[-60, -20]$ dB and $[-\pi, \pi]$, respectively. Moreover, for Canc-DL-R and Canc-DL-C, we consider *DL step size* of $\tau_\Delta \in \{0.5, 1.0, \ldots, 5.0\}$ ns, i.e., an N^{dl}-tap time-domain RF canceller is associated with DL values of $\boldsymbol{\tau} = [0, \tau_\Delta, \ldots, (N^{\text{dl}} - 1)\tau_\Delta]$.[2] For Canc-BPF, we consider *BPF center frequency tuning range to bandwidth ratio* of $\gamma \in \{0.2, 0.4, \ldots, 2.0\}$, i.e., $f_{\text{c},n} \in \{f_{\text{carr}} - \frac{\gamma B}{2}, f_{\text{carr}} + \frac{\gamma B}{2}\}$. In addition, we set the quality factor tuning range as $Q_n \in [10, 50]$.

In the *practical case with quantizations*, we apply a 0.25 dB resolution to the amplitude tuning, and an 8-bit resolution to the phase, center frequency, and quality factor tunings (i.e., 256 equally spaced values for each parameter). These tuning ranges and resolutions are practically selected and can be easily implemented as described in [43]. It is expected that better resolutions of these configuration parameters can result in smaller performance degradation compared to the ideal case. Note that the effect of the amplitude/phase tuning resolution on the achievable SIC using a single-tap canceller in a narrowband setting has been analyzed in [105]. However, its extension to wideband scenarios with multi-tap cancellers is non-trivial and thus, is considered as future research.

In Sections VI-B and VI-C, we present the performance of RF SIC under the MMSE-based algorithm (see Section V-A), where the RF canceller configuration parameters in the ideal case are obtained using the nonlinear solver in MATLAB. These parameters are then rounded to their closest quantized values in the practical case. In Section VI-D, we also use examples to illustrate the performance of the DLS algorithm (see Section V-B) and its comparison to the MMSE-based algorithm. Note that in this paper, we focus on the fundamental limits of the achievable RF SIC, and the tuning algorithm can be implemented more efficiently (e.g., on an FGPA/embedded platform with code optimization) based on the specific RF canceller hardware.

[1]While the RF SIC performance can potentially be further increased with a larger value of $N^{\text{dl/bpf}}$, we consider these values of $N^{\text{dl/bpf}}$ based on the configuration and range limit of the measurement equipment.

[2]This also includes the *reconfigurable* time-domain RF cancellers where the tunable DL taps are configured using τ_Δ.

B. RF SIC Achieved by Time-Domain RF Cancellers

Fig. 6 plots the RF SIC achieved by time-domain RF cancellers under three antenna interfaces with varying bandwidth, B, number of DL taps, N^{dl}, and DL step size, τ_Δ. In particular, we consider up to 128 and 64 taps for Canc-DL-R and Canc-DL-C, respectively, so that they have the *same* total number of DoF (see Table II). The results show that for Canc-DL-R, the DL step size needs to be carefully selected based on the antenna interface in order to achieve good RF SIC performance, as was done in [7]. This limitation is relaxed for Canc-DL-C, where phase tuning is introduced for each DL tap. Take Ant 3 with 1 ns DL step size and 120 MHz bandwidth as an example: for Canc-DL-R with 8/16/32 taps, the achievable RF SIC in the ideal and practical case is 18.1/29.1/43.1 dB and 17.8/26.6/24.5 dB, respectively. For Canc-DL-C with 4/8/16 taps, the achievable RF SIC in the ideal and practical case is 30.8/42.8/48.4 dB and 26.6/32.2/30.2 dB, respectively. It can be seen that with the same total number of DoF (see Section VI-A), Canc-DL-C with complex-valued weights achieves on average better performance than Canc-DL-R with real-valued weights.

More importantly, for the considered antenna interfaces and canceller settings, a larger value of N^{dl} *does not* significantly improve the performance of RF SIC. As an example, for Ant 2 with 2 ns DL step size and 120 MHz bandwidth, Canc-DL-C achieves 38.1/44.3 dB RF SIC with only 8/16 taps, while the performance is improved to 53.4 dB with 64 taps. Even in the practical case with quantization constraints, 8/16/64 DL taps can achieve an RF SIC of 37.9/38.9/39.9 dB. This is because with a fixed DL step size, an increased number of DL taps only allows the canceller to capture a larger delay value in the SI channel. However, if more DL taps are introduced within the same range of delay values (i.e. with a higher DL resolution), the canceller will be able to better reconstruct the SI signal to improve the SIC performance. In addition, how well the SI signal can be reconstructed by a canceller depends on the hardware quantization and resolution, which can potentially further limit the achievable SIC. Note that similar results can be obtained from Fig. 6 with Ant 1 and Ant 3. These results provide insights on the design of time-domain RF cancellers taking into account the tradeoffs between the hardware complexity and achievable RF SIC performance.

C. RF SIC Achieved by Frequency-Domain RF Cancellers

Fig. 7 plots the RF SIC achieved by frequency-domain RF cancellers under three antenna interfaces with varying bandwidth, B, number of BPF taps, N^{bpf}, BPF center frequency tuning range to bandwidth ratio, γ. In particular, we consider $N^{\text{bpf}} \in \{2, 4, \ldots, 32\}$ so that has the *same* total number of DoF compared with Canc-DL-R and Canc-DL-C (see Table II). In particular, we consider up to 32 BPF taps for Canc-BPF so that it has the *same* total number of DoF compared with the Canc-DL-R and Canc-DL-C described above in Section VI-C (see also Table II).

The results show that in order to achieve a sufficient amount of RF SIC, γ needs to be at least around 0.5–1.0 (i.e., the BPF center frequency tuning range needs to be comparable

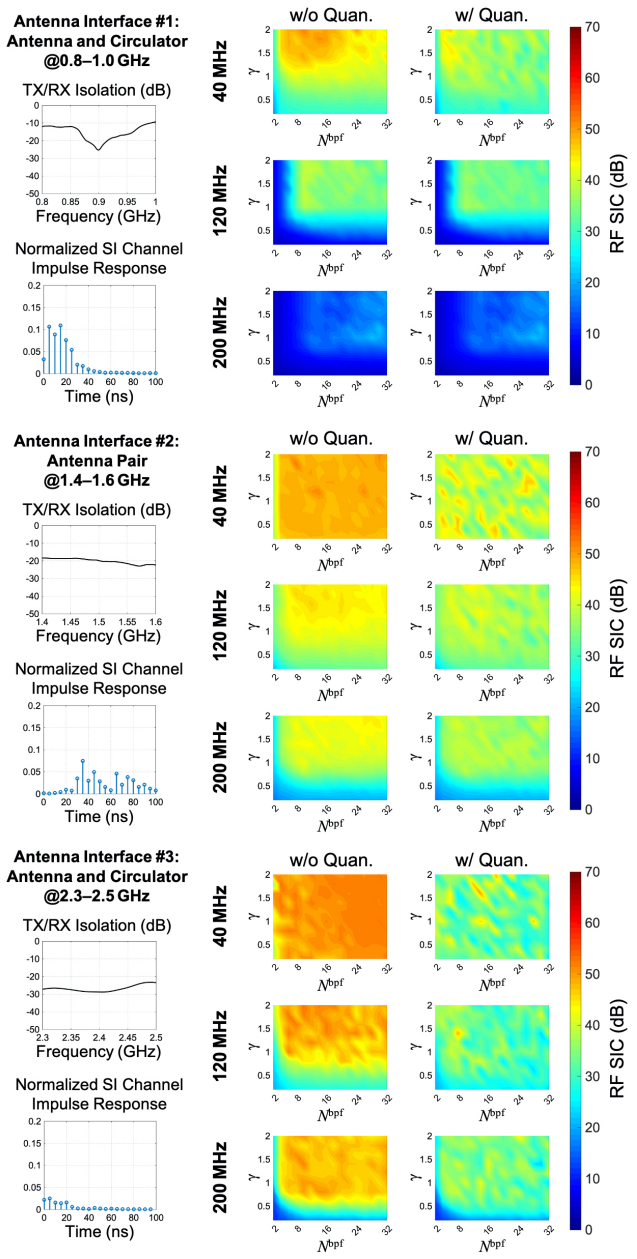

Fig. 7: Numerical evaluations of the achievable RF SIC using the frequency-domain approach employing reconfigurable bandpass filter (BPF) taps (**Canc-BPF**), with varying number of BPF taps, N^{bpf}, BPF center frequency tuning range to bandwidth ratio, γ, three antenna interfaces (**Ant 1**, **Ant 2**, and **Ant 3**) at different frequencies, f_{carr}, and RF SIC bandwidth, B, in both the ideal (without quantizations) and practical (with quantizations) case.

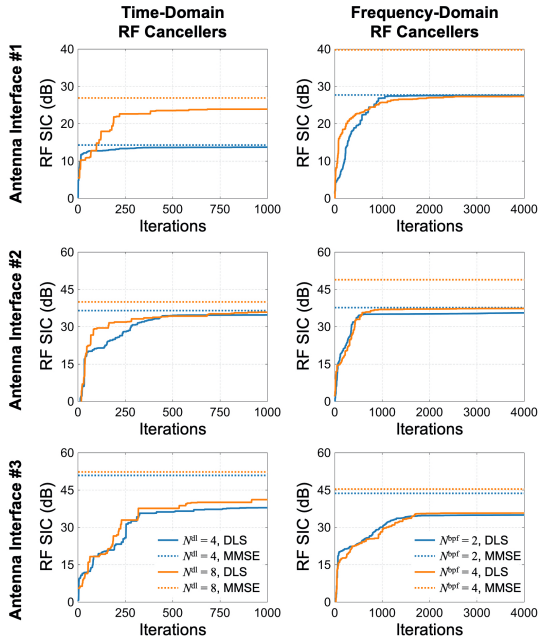

Fig. 8: Numerical evaluation of the achievable RF SIC under both the DLS (solid lines) and MMSE-based (dashed lines) algorithms, with two types of RF cancellers, three antenna interfaces at different frequencies, and 40 MHz bandwidth, in the ideal case. The considered time-domain RF canceller is **Canc-DL-C** with 4/8 taps and 2 ns delay line resolution, and the frequency-domain RF canceller is **Canc-BPF** with 2/4 taps and $\gamma = 1$.

to the signal bandwidth). For example, with Ant 3, $\gamma = 1$, and 120 MHz bandwidth, the RF SIC achieved by Canc-BPF with 2/4/8 BPF taps in the ideal and practical case is 24.3/37.8/47.6 dB and 24.3/34.9/37.8 dB, respectively. The performance is comparable to that achieved by Canc-DL-C with the same total number of DoF (see Section VI-B).

Similar to the case of Canc-DL-R and Canc-DL-C, a larger value of N^{bpf} does not significantly improve the performance of RF SIC. For example, with Ant 2, $B = 120$ MHz, and $\gamma = 1$, Canc-BPF achieves 33.8/37.1 dB RF SIC with only 2/4 taps, while the performance is improved to 41.0 dB with 32 taps. Even in the practical case with quantization constraints, Canc-BPF with 2/4/32 BPF taps achieves an RF SIC of 33.0/36.3/39.8 dB.

In general, it is challenging to make a conclusion on which type of canceller will have better RF SIC performance. Despite the different hardware implementations, even with a given antenna interface, the corresponding SI channel profile can be time-varying and dependent on the dynamic environmental effects. In order to achieve the best canceller performance, it is required that the canceller can be tuned in a practical setting (with practical hardware impairments and quantization constraints) so that its frequency response matches best with that of the SI channel. As illustrated in Figs. 6 and 7, for the same antenna interface with reasonable tuning ranges of the parameters, the considered time- and frequency-domain cancellers with a similar total number of DoF can achieve comparable SI cancellation performance.

D. RF Canceller Tuning Algorithms: MMSE vs. DLS

We implement and evaluate the DLS algorithm for Canc-DL-C and Canc-BPF with 4/8 taps and 2/4 taps, respectively (with a total number of DoF $M \in \{8, 16\}$), and compare its performance with that achieved by the MMSE-based algorithm. We consider the same three antenna interfaces and generate the dither signal in each iteration as described in Section V-B with a step size of $\mu = 0.05$. Fig. 8 presents the RF SIC achieved by the DLS algorithm over iterations (solid lines) and by the MMSE-based algorithm (dashed lines).

In particular, the results for the MMSE-based algorithm are obtained as the final solution to (7) returned by the `fmincon` nonlinear programming solver in MATLAB with the default settings. The results for the DLS algorithm are obtained using a customized MATLAB implementation.

As described in Section V-B, DLS runs efficiently since it requires only the residual SI power measurements and involves no complex optimization. For example, one iteration takes less than 10 μs in our MATLAB implementation on a laptop with a quad-core Intel i7 CPU, and the computation time can be significantly improved using a C++/FPGA implementation. In general, DLS achieves good performance with a smaller number of canceller taps (equivalently, DoF). For example, for Canc-DL-C/Canc-BPF with 4/2 taps with **Ant 1**, DLS converges to within 1% of the performance achieved by MMSE in less than 1,000 iterations (i.e., less than 10 ms). However, it can also be seen that the performance of DLS depends on different antenna interfaces and canceller setups, and degrades with an increasing number of canceller taps. This is mainly due to the fact that, as shown in (8), the dithered signal $\mathbf{d}$, is generated using a uniform distribution with zero mean, and all the canceller parameters are perturbed using the same scaling factor, which does not distinguish the difference between different types of configuration parameters (e.g., the amplitude and phase of a delay time tap). Improving the performance of the DLS algorithm with a larger number of canceller taps is a subject of our future research directions.

VII. Implementations and Experimentation

As mentioned in Sections III and IV, both time- and frequency-domain RF cancellers have been realized and demonstrated at the system-level (see also Table III). In this section, we briefly present two SI canceller implementations based on our recent work: a time-domain canceller with 16 RF taps and 8 analog BB taps, and a frequency-domain canceller with 2 RF BPF taps. The implementation details and more comprehensive performance evaluations can be found in [43], [44], [66], respectively.

A Time-Domain Canceller With Reconfigurable RF and Analog Baseband Taps: In [44], we presented a 0.1–1.0 GHz FD receiver that integrates time-domain RF and analog BB cancellers (see Fig. 9(a) for the chip microphotograph). The RF canceller consists of 16 RF DL taps with programmable delay values implemented using multipath switched-capacitor-based delays with a delay range of 0–8.5 ns (see Fig. 9(b) for the measurement results), and each tap is associated with a 6-bit amplitude control. In this implementation, the input signal is periodically sampled onto a capacitor and the stored sample is sensed at the output through a switch controlled by a delayed version of the sampling clock thus imparting the delay between the clocks to the two sets of switches to the input signal. These switched-capacitor-based delays require a single additional clock whose frequency can be programmed to change the delay resolution obtained from these taps. Furthermore, the DL value of each tap can be programmed using an on-chip MUX which shifts the clock phases driving the two sets of switches. The BB canceller is implemented using 8 analog BB DL taps

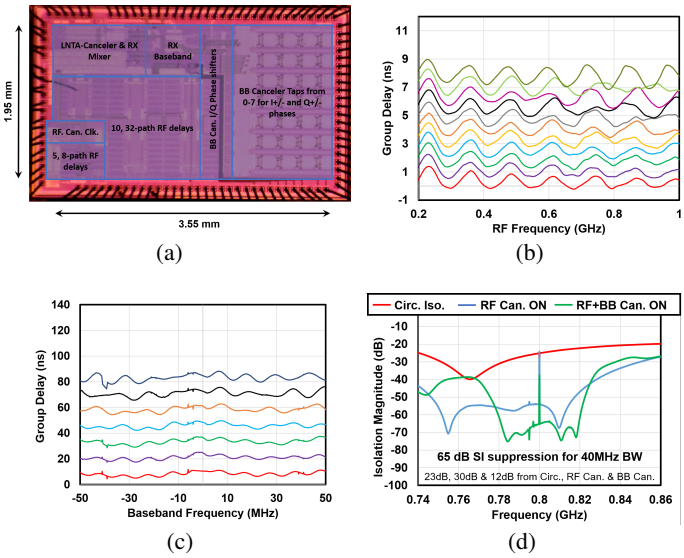

Fig. 9: (a) Chip microphotograph of the implemented wideband FD receiver integrating an RF canceller with 16 reconfigurable DL taps and a BB canceller with 8 DL taps [44], (b) measured individual RF tap delays of to 8 ns delay, (c) measured individual analog BB tap delays of up to 85 ns, and (d) measured SIC in the RF and analog BB domains with +15 dBm TX power and 40 MHz bandwidth.

with similar switched capacitor networks and has a delay range of 0–85 ns (see Fig. 9(c) for the measurement results), and each tap is associated with 7-bit amplitude control. With a realistic antenna interface at 800 MHz operating frequency, the weights of this canceller are optimized using the MMSE-based tuning algorithm, and Fig. 9(d) shows the measured SIC performance achieved by this canceller. By virtue of the higher delay range obtained in the RF domain, 30/12 dB SIC is achieved in the RF/analog BB domain across 40 MHz bandwidth, which is a significant improvement compared with that reported in [46]. This improved canceller can handle up to +15 dBm average TX power with a DC power consumption of 44.8 mW.

A Frequency-Domain RF Canceller with 2 BPF Taps: In [66], we designed and implemented a 0.8–1.4 GHz FD receiver with an integrated frequency-domain RF canceller in the 65 nm CMOS process (see Fig. 10(a) for the chip microphotograph), which achieves 20 dB RF SIC across 25 MHz bandwidth. To facilitate easy integration with a software-defined radio (SDR) platform and research on the higher networking layers, in [43] we implemented a frequency-domain RF canceller consisting of 2 reconfigurable BPF taps using discrete components on a PCB (see Fig. 10(b)), which emulates its IC counterpart [66]. We also prototyped wideband FD radios using this RF canceller and NI USRP SDRs (see Fig. 10(c)), which operate at around 900 MHz carrier frequency.

We implemented a full OFDM-based Physical (PHY) layer with a real-time RF bandwidth of 20 MHz using NI LabVIEW, supporting various modulation and coding schemes. The digital SIC algorithm is also implemented to further suppress the residual SI signal after RF SIC, which is based on Volterra series and a least-square problem similar to that presented

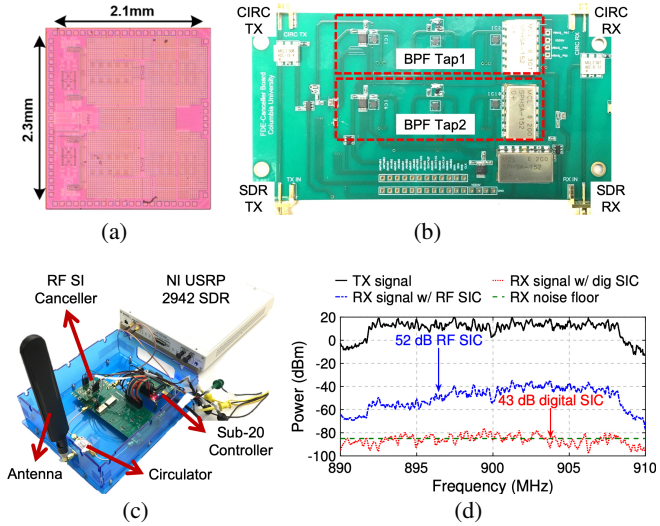

Fig. 10: (a) Chip microphotograph of the implemented 0.8–1.4 GHz 65 nm CMOS FD receiver with a frequency-domain RF SI canceller featuring two BPFs [66], (b) the implemented frequency-domain RF canceller with 2 reconfigurable BPF taps on a PCB [43], which emulates its RFIC counterpart in (a), (c) the prototyped wideband FD radio consisting of an antenna, a circulator, a frequency-domain RF SI canceller, and a USRP SDR, and (d) power spectrum of the received signal after SIC in the RF and digital domains with +10 dBm average TX power, 20 MHz bandwidth, and −85 dBm RX noise floor.

in [7]. Fig. 10(d) shows the node-level measurement results of the FD radio achieving 95 dB overall SIC across 20 MHz, where 20/32/43 dB is achieved at the antenna interface and in the RF/digital domain, respectively. Since the USRP has a noise floor of −85 dBm (limited by the environmental interference at around 900 MHz), the FD radio can support an average TX power of +10 dBm with a peak TX power of +20 dBm.

In addition, despite extensive research in this area, an open-access wireless testbed with FD-capable nodes is still needed for experimental evaluations of FD-related algorithms at the higher layers. To allow the broader community to experiment with FD, we integrated the wideband FD radios in the NSF PAWR COSMOS testbed [71], [106], [107], which is a programmable city-scale advanced wireless testbed currently being deployed in West Harlem, New York City. These are the *world's first open-access wideband FD radios that are remotely accessible*.[3]

VIII. Challenges and Future Directions

In this paper, we provided a comprehensive overview and comparison of recent advances in IC-based shared antenna interface and RF/analog BB canceller implementations, which are critical components for realizing the full potential of FD in mobile/hand-held devices. We defined two figures of merit (FOM) for integrated antenna interfaces and cancellers that capture various design and performance tradeoffs including the amount of TX-RX isolation/SIC and bandwidth, TX/SI power handling, noise figure degradation, and power consumption. We also took an overarching approach to presenting the models of and comparison between two types of SI cancellers using time- and frequency-domain approaches, and two canceller tuning algorithms. We numerically evaluated the performance of these cancellers in different scenarios, and presented an overview of three of our IC-based canceller implementations. We believe that these results can provide insights into the design of RF cancellers with different hardware constraints and performance requirements.

Looking forward, improving the antenna interface and canceler efficiencies (η_{ANT} and η_{CANC}) by reducing their insertion losses and DC power consumption will be an important research direction. Additionally, the design and implementation of these integrated RF and/or analog BB cancellers with a large number of taps (e.g., 32 or 64) requires significant research efforts on the hardware level. These cancellers will have the capability to achieve further improved SIC over a larger signal bandwidth thereby improving the SIC-FBW product. More efficient and adaptive canceller tuning algorithms, potentially leveraging machine learning techniques, are needed to achieve improved performance of both types of cancellers. Such adaptive algorithms are particularly important for cancellers with a large number of taps, whose total number of possible configurations grow exponentially as a function of the number of configuration parameters. In addition, the co-design and joint optimization of cancellers across different domains (e.g., between RF and analog/digital baseband) are necessary for advancing both single- and multi-antenna FD systems.

Moreover, there are open problems related to obtaining a better understanding of the interactions between the PHY layer implementations and higher layer protocols/applications in different networking scenarios (e.g., interference management, resource allocation [108], scheduling [109], and use of FD in integrated access and backhaul [IAB] systems [110]). We believe that by bridging the knowledge from the antenna design, microwave theory, IC, communication/information theory, and wireless networking communities, we will be able to identify and address these challenges using a holistic interdisciplinary and cross-layered approach.

[3]The detailed tutorial and open-source code are available at https://wiki.cosmos-lab.org/wiki/Tutorials/Wireless/FullDuplex.

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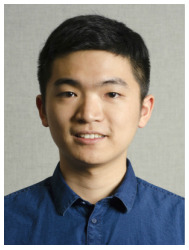

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