6.6 Full-Duplex Receiver with Wideband Multi-Domain FIR Cancellation Based on Stacked-Capacitor, N-Path Switched-Capacitor Delay Lines Achieving >54dB SIC Across 80MHz BW and >15dBm TX Power-Handling

Aravind Nagulu*[1], Sasank Garikapati*[1], Mostafa Essawy[2], Igor Kadota[1], Tingjun Chen[1], Arun Natarajan[2], Gil Zussman[1], Harish Krishnaswamy[1]

[1]Columbia University, New York, NY
[2]Oregon State University, Corvallis, OR

*Equally-Credited Authors (ECAs)

2021 IEEE International Solid- State Circuits Conference (ISSCC) | 978-1-7281-9549-0/20/$31.00 ©2021 IEEE | DOI: 10.1109/ISSCC42613.2021.9365947

Full-duplex (FD) transceivers remain a significant challenge as they require >100dB of cancellation of high levels of self-interference (SI), recreation of large SI channel delay spreads, and real-time canceler adaptation. SI cancelers based on frequency-domain equalization (FDE) [1,2] demand multiple widely-tunable power-hungry high-Q filters, while those based on FIR-based time-domain equalization (TDE) [3-5] require large delays with fine resolution (see Fig. 6.6.1 for a system simulation based on the isolation profile of an SI channel, where the TX-RX leakage spreads across several 10s of nano-seconds). Additionally, supporting realistic antenna interface isolations of ~20dB requires a low-loss canceler and stresses canceler noise and linearity [6]. This work introduces - (i) an N-path switched-capacitor (SC) delay-line with stacked-capacitor voltage gain while enabling nearly ten nanoseconds of RF true-time delay across a large BW (DC to 1GHz), (ii) a new LNTA canceler where the FIR weighting, summation, and output buffer of the canceler is absorbed into the LNTA, and (iii) a closed-loop adaptation algorithm leveraging analytical modeling of tap non-idealities that reduces the computational complexity and data storage. Leveraging a 16-tap RF canceler operating across DC to 1GHz with delays ranging from 0.25ps to 8ns (8× compared to [5] and 40× compared to [4]) and a complex-weighted 8-tap BB canceler with delays ranging from 10ns to 85ns, the FD receiver achieves (i) tunable operation across 200MHz to 1GHz, (ii) wideband SI suppression of up to 65dB (54dB) across 40MHz (80MHz), when operating at 800MHz (13dB higher than [5] while achieving 2× cancellation BW), with (iii) modest NF degradation of 0.8dB (2.8dB) for the low-power mode (high-power mode), while (iv) handling TX power of up to +15dBm (6dB higher than [5]) across an initial circulator isolation of only 23dB (11 to 18dB better than [1-4]).

Delays based on the sample-hold-and-release principle of SC circuits [5] can enable large delays ($\propto 1/f_s$ over antialiasing BW=$f_s/2$) within a compact area. By staggering the input (charging) and output (discharging) phases by $\Delta\tau$, a true time delay determined by the clocks can be achieved. Additionally, the BW can be enhanced to $Nf_s/2$ by using a time-interleaved N-path structure as in Fig. 6.6.1. Switch parasitics and rise/fall time of the clocks results in additional losses, compromising the power handling. Active gain adds additional noise, distortion and DC power. We propose capacitor-stacking to achieve passive voltage gain in the canceler delay line. In this scheme, multiple capacitors are charged in parallel from the input, and during the discharge phase, are stacked upon each other, resulting in voltage gain.

A TDE FIR canceler requires FIR weighting, summation, and injection into the RX. Our new LNTA canceler (Fig. 6.6.2) absorbs these functions into the LNTA, resulting in a lower NF by up to 1dB. The LNTA canceler follows the partial-noise-canceling LNTA, where a part of the current from the tail transistor is steered back to the RX input through a common-gate (CG) device to provide wideband input matching and partial noise cancellation. Driving the gate of the CG device with an appropriately scaled SI replica results in a cancellation path that provides partial SI cancellation at the input of the LNTA of ~$1/N$ (-15dB in our implementation), where N>>1 is the ratio of the output current to the steered-back current, and a complete suppression of the SI current at the LNTA output. The CG device is split into 16 segments, whose gates are connected to the outputs of the delay taps. By segmenting and individually controlling these CG slices further, FIR weighting is achieved. At low SI levels, the weights are chosen for minimal NF degradation (low-power (LP) mode). At high SI levels, larger weights are chosen for up to 6dB higher SI power handling in the RF canceler (high-power (HP) mode) at the expense of 2dB NF degradation.

Figure 6.6.2 shows the circuit diagram of the FD RX. TX power is capacitively coupled to the RF canceler, and then fed to the delay taps by source-follower buffers. System analysis reveals that while the overall SIC is a function of both the canceler delay resolution ($\Delta\tau$) and the maximum delay ($N\Delta\tau$), only a fraction of the total N taps are used in any given situation. Therefore, we implemented a 16-tap RF canceler with 32 possible delay settings, namely 1 zero-delay tap, 5 low-delay, 8-path delay taps with $f_{s,RF8}$=500MHz, and 10 high-delay, 32-path delay taps with $f_{s,RF32}$=125MHz. Each of the 8-path (32-path) delays can be programmed to one of the delays ranging from $T_{s,RF8}/8$ to $7T_{s,RF8}/8$ ($T_{s,RF32}/32$ to $31T_{s,RF32}/32$), resulting in delays of 250ps to 1.75ns (250ps to 7.75ns). The 2-stage capacitive stacking results in a passive voltage gain of 6 to 4dB across DC to 1GHz. The BB canceler consists of a 4-phase I/Q down-mixer, followed by I/Q BB TIAs. These are followed by 4 sets of 1 zero-delay tap and 7 8-path SC delay taps with increasing phase staggering resulting in delays ranging from $T_{s,BB}/8$ to $7T_{s,BB}/8$. Due to the low BB frequencies, these taps can be clocked at much lower frequencies (e.g. 10MHz) to realize large delays (12.5ns to 87.5ns with 12.5ns step). The I/Q outputs of the BB delay taps are then passed to vector modulators performing complex weighting, and are injected into the RX chain at the outputs of the RX mixers.

The 65nm CMOS FD receiver occupies a chip area of 3.55mm×1.55mm (Fig. 6.6.7). The wideband RX shows conversion gain of 15 to 40dB (24dB nominal), NF of 3.7dB, IIP3 of -14dBm, and IP_{1dB} of –25dBm while consuming 34mW. Figure 6.6.3 shows the magnitude and group delay profiles of an 8-path RF delay tap across its 7 possible delays, a 32-path RF delay tap across 11 of all possible 31 delays, and the BB canceler delay taps for $f_{s,BB}$ = 10MHz and 20MHz. The losses include the attenuation due to the high-impedance TX-sensing and feed-in to the RX input, so these cancelers can handle antenna isolation levels of ~20 to 25dB. The flatness over any <80MHz band is sufficient for true FIR behavior, while the flatness over DC to 1GHz is sufficient for reconfigurable operating frequency. Due to the co-designed LNTA-canceler architecture, we measured the RF delay taps from the TX port to the RX input through the LNTA canceler which added additional dispersion to the measurements in Fig. 6.6.3. For these switching frequencies, the RF and BB canceler taps consume 7.4mW and 1.9mW per tap, respectively. We co-optimized the SIC with the NF degradation though a closed-loop algorithm depicted in Fig. 6.6.5 that leverages a one-time calibrated, analytical model for each tap that captures measured systematic and random tap non-idealities and tap-to-tap variation to greatly reduce computation and storage requirements by 100× when compared with a brute force approach that uses full measurements of all taps. This iterative closed loop can, in principle, also be expanded to account for variations with temperature and supply voltage. For a BW of 40MHz, measured SIC for two different circulator-based antenna interfaces operating at 800MHz and 460MHz is 65dB (23dB, 30dB & 12dB from circulator, RF canceler and BB canceler) and 57dB (22dB, 25dB & 10dB from circulator, RF canceler and BB canceler) respectively (Fig. 6.6.4). At 800MHz (460MHz), we measured a total SI suppression of 65, 65, 57 and 54dB (67, 57, 52 and 45dB) across a BW of 20, 40, 60 and 80MHz respectively. Under this cancellation, the NF degradation from the RF and BB canceler is 0.3dB and 0.5dB on top of a baseline RX NF of 3.7dB. These SIC levels remain consistent across TX power levels of up to +7dBm (-15dBm at RX input). For TX power exceeding +7dBm, we switch to HP mode with an additional 2dB NF degradation. In HP mode, a TX power of +15dBm (-7dBm at the RX input) can be handled without compressing the receiver. Figure 6.6.5 shows a total SI suppression of 47dB across 80MHz when the circulator is terminated with a COTS antenna using the closed-loop SIC calibration algorithm. Figure 6.6.5 also confirms that for the 460MHz circulator, the SIC achieved by the closed-loop algorithm based on analytical modeling shows no degradation compared to the brute-force approach. Figure 6.6.6 shows the performance comparison with prior art. Compared to the prior TDE (FDE) cancelers, we achieve 15dB (25dB) higher SIC for similar fractional BW and +6dB (+1dB) higher TX power handling with 0.7dB (0.2dB) better overall NF.

Acknowledgement:
This work was supported by DARPA SPAR, SRC-DARPA ComSenTer center, and NSF grant ECCS-1547406.

References:

[1] J. Zhou et al., "Receiver with >20MHz Bandwidth Self-Interference Cancellation Suitable for FDD, Co-existence and Full-Duplex Applications," *ISSCC,* pp. 342-343, Feb. 2015.

[2] T. Chen et al., "Wideband Full-Duplex Wireless via Frequency-Domain Equalization: Design and Experimentation," *ACM MobiCom,* pp. 1-16, Aug. 2019.

[3] T. Zhang et al., "A 1.7-to-2.2GHz Full-Duplex Transceiver System with >50dB Self-Interference Cancellation Over 42MHz Bandwidth," *ISSCC*, pp. 314-315, Feb. 2017.

[4] K. Chu et al., "A Broadband and Deep-TX Self-Interference Cancellation Technique for Full-Duplex and Frequency-Domain-Duplex Transceiver Applications," *ISSCC*, pp. 170-171, Feb. 2018.

[5] A. Nagulu et al., "A Full-Duplex Receiver Leveraging Multiphase Switched-Capacitor-Delay Based Multi-Domain FIR Filter Cancelers," *IEEE RFIC,* pp. 43-46, Virtual, Aug. 4-6, 2020.

[6] J. Zhou et al., "Integrated Full Duplex Radios," *IEEE Communications Magazine*, pp. 142-151, April 2017.

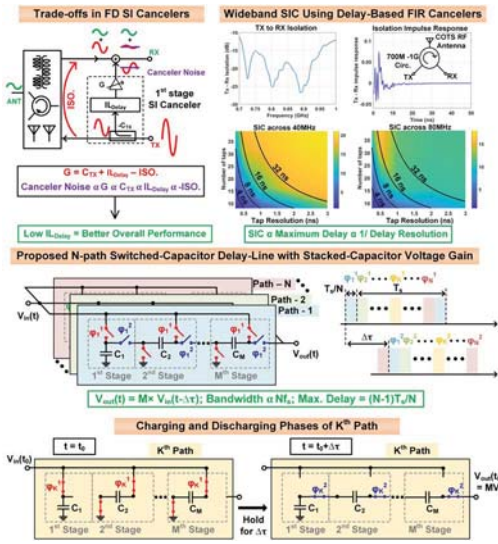

Figure 6.6.1: Trade-offs and requirements on FD SI cancelers to achieve wideband self-interference cancellation, and proposed N-path, switched-capacitor delay line with stacked-capacitor voltage gain.

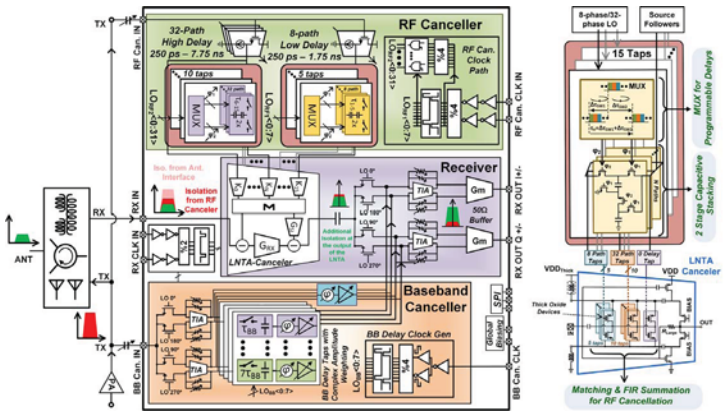

Figure 6.6.2: Block and circuit diagram of the 200MHz-to-1GHz FD RX performing multi-domain SI cancellation through a 16-tap RF FIR canceler, an LNTA-canceler with embedded FIR weighting and summation, and an 8-tap complex-weighted BB FIR canceler.

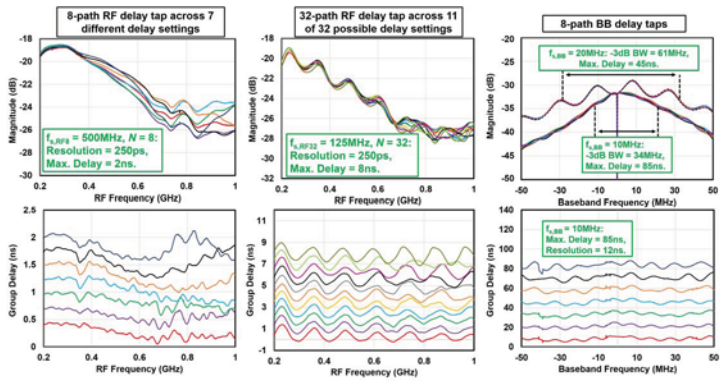

Figure 6.6.3: Measured performance of the cancelers: magnitude and group delays of an 8-path delay tap and a 32-path delay tap of the RF canceler, and an 8-path delay tap of the BB canceler across various possible delay settings. The losses in these graphs include the attenuations due to the high-impedance TX-sensing and feed-in to the RX input.

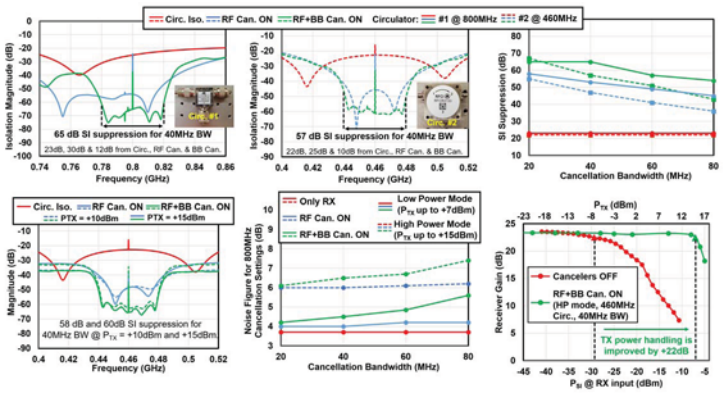

Figure 6.6.4: Measured FD performance: SI suppression at two different frequencies with two different circulators (460MHz and 800MHz), SI suppression vs. the cancellation bandwidth, SI suppression at high PTX powers when operated in HP mode, noise-figure degradation vs. cancellation BW in LP and HP modes, and power handling referenced to RX input and TX input.

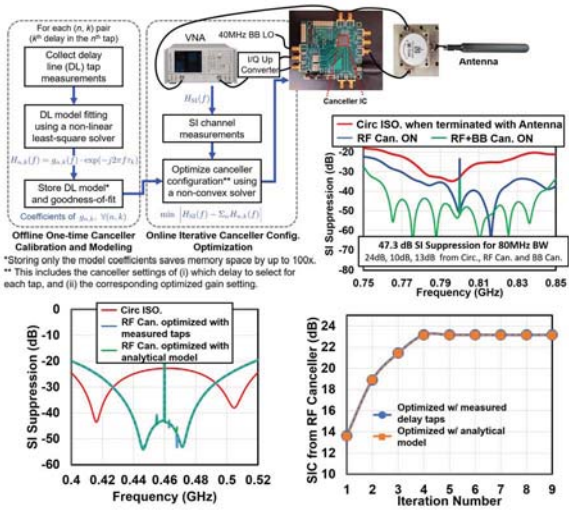

Figure 6.6.5: Closed-loop SIC calibration algorithm leveraging analytical modeling of tap non-idealities greatly reduces the computational complexity and data storage requirements of the SIC optimization. 47dB SI suppression across 80MHz is achieved when the 800MHz circulator is terminated with a COTS antenna.

		ISSCC 2015 [1]	ISSCC 2017 [3]	ISSCC 2018 [4]	RFIC 2020 [5]	This Work
	Architecture	RX with wideband SIC based on RF frequency-domain equalization	Adaptive Filter + Noise Canceling PA + LO sideband suppression	Electrical Balance Duplexer + Double-RF Adaptive FIR Filter	RX with SIC in RF and BB domains with switched capacitor FIR filters	RX with SIC in RF and BB domains using stacked-capacitor switched-capacitor FIR filters and an embedded LNTA-canceler
RX metrics	RX Frequency Range	0.8GHz - 1.4GHz	1.7GHz - 2.2GHz	1.6GHz - 1.9GHz	0.1GHz - 1GHz	**0.1GHz – 1GHz**
	Gain	27dB - 42dB	20dB - 36dB	42dB	15 – 38dB	**15 - 40dB**
	Noise Figure	4.8dB	4dB	8.1dB	5.3dB	**3.7dB**
	In band IIP3/IIP1dB	-20dBm/-30dBm [a]	-5dBm/-15dBm [a]	N/R	-18.7dBm/-27dBm (for Gain of 27dB)	**-14dBm/-25dBm (for Gain of 24dB)**
FD Metrics	Integrated SIC Domains	RF	RF + BB	RF	RF + BB	**RF + BB**
	Canceler delay	RF - 1ns to 29ns [a]	RF - 0 to 0.26ns BB - 0 to 130ns	RF - 0 to 0.2ns, BB - N/A	RF – 0.2ns to 1.1ns BB – 10ns to 75ns	**RF – 0 to 7.75ns BB – 0 to 85ns**
	Complex Canceler Gains	RF – Yes	RF – No BB –Yes	No	RF – No BB –Yes	**RF – NO BB – Yes**
	Delay Programmability	Yes	No	No	No	**Yes**
	Number of taps in Canceler	RF - 2 bandpass filters	RF - 5 BB - 14	RF - 5 BB - N/A	RF - 7 BB - 7	**RF - 16 BB – 8**
	Initial TX-RX isolation	>34dB (antenna pair)	30dB - 35dB (off-chip circ., 50Ω)	26dB (on chip EBD, 50Ω)	22dB / 21 dB (off-chip circ. 50Ω / antenna)	**22 - 23dB (off-chip circ. 50Ω / antenna)**
	SIC from the Cancelers [a] (Not including Ant. ISO.)	18MHz (1.3%) for 20dB (1 filter) 26MHz (1.9%) for 20dB (2 filters)	42MHz (2.1%) for 50dB	20MHz (1.1%) for 33.8dB 40MHz (2.2%) for 31.1dB 80MHz (4.4%) for 26.2dB	20MHz (2.7%) for 29dB	**40MHz (5%) for 42 dB @ 800MHz 40MHz (8.7%) for 35 dB @ 460MHz**
	NF degradation	0.9dB - 1.2dB (one filter) 1.1dB - 1.5dB (two filters) (for >34dB initial isolation)	1.55dB (for 30-35 dB initial isolation)	1.6dB (for 39dB initial isolation)	1.1 dB from RF Canceler 0.8 dB from BB Canceler (for 22dB initial isolation)	**RF Can. LP (HP) modes: 0.3dB (2.3dB) BB Can. LP(HP) modes: 0.5dB (0.8dB) (23dB Ant. ISO. and 40MHz BW)**
	SI Power Handling Referenced to RX Input	-8dBm	N/R	N/R	-13dBm	**-12dBm (LP mode) -7dBm (HP mode)**
	RX Power	63mW - 65mW	22mW	82.3mW	31mW	**34mW**
Others	Canceler Power	88mW - 192mW	3.5mW (RF) + 8mW (BB)	14.3mW	25.5mW (RF) 6.5mW (BB)	**7.4mW per tap (RF) 1.5mW per tap (BB)**
	Technology	65nm CMOS	40nm CMOS	40nm CMOS	65nm CMOS	**65nm CMOS**
	Active Area	4.8mm²	3.5mm²	4mm²	5.15mm²	**7.2mm²**

[a] - Found in the journal version of their work. [b] - Narrowband delay due to bandpass filter(s). [c] - Fractional BW is calculated from the frequency of measured isolation. N/A – Not Applicable. N/R – Not reported.

Figure 6.6.6: Performance summary and comparison table of integrated, single-antenna FD systems.

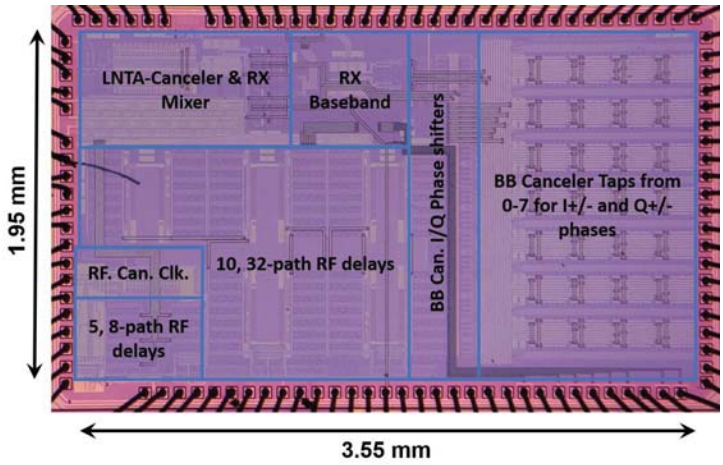

Figure 6.6.7: Die micrograph.

978-1-7281-9549-0/21/$31.00 ©2021 IEEE