Demo: Experimentation with Wideband Real-Time Adaptive Full-Duplex Radios

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ABSTRACT

We present a set of experiments utilizing *wideband real-time adaptive* full-duplex (FD) radios, demonstrating simultaneous transmission and reception on the same frequency channel. Each FD radio consists of a circulator-based antenna interface, a switched-capacitor delay-line-based configurable Radio-Frequency Integrated Circuit (RFIC) that implements Self-Interference Cancellation (SIC), an FPGA that optimizes the RFIC configuration in under 1.1 sec and can adapt to environmental changes in under 0.3 sec, and a Software-Defined Radio (SDR) transmitting OFDM-like packets. We demonstrate a real-time adaptive FD radio that achieves the SIC necessary to reach the noise floor across a wide bandwidth of 50 MHz. Then, we use two FD radios to create a wireless link and showcase the superior FD throughput.

CCS CONCEPTS

• **Hardware** → **Wireless devices**; *Radio frequency and wireless circuits*; • **Networks** → **Network architectures**; **Network experimentation**; **Wireless access networks**.

KEYWORDS

Full-Duplex Wireless, Real-Time Adaptation, Self-Interference Cancellation, Software Defined Radio

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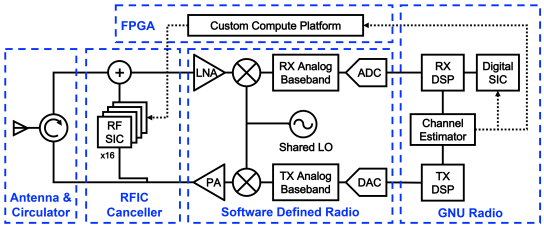
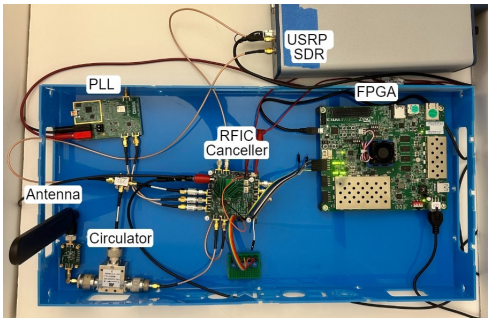
1 INTRODUCTION

Full-duplex (FD) wireless has drawn significant attention in recent years [3, 16, 17, 22] as an enabler of next-generation wireless networks, due to its potential to double the data rate at the Physical layer (PHY) and to provide additional cross-layer benefits throughout the networking stack. The main challenge associated with FD wireless is the strong self-interference (SI) signal at the receiver that needs to be suppressed to the noise floor, requiring 70 – 110 dB of SI cancellation (SIC) across the antenna, analog, and digital domains.



(a) Block diagram of the presented FD radio.



(b) Implementation of the presented FD radio.

Figure 1: The wideband real-time adaptive FD radio consisting of an antenna, a circulator, an RFIC canceller, an SDR, a PC running GNU Radio, and an FPGA. A phase-locked loop (PLL) synthesizer provides the clocks used by the RFIC.

Achieving sufficient SIC is a challenge even at relatively narrow bandwidths (i.e., ≤ 20 MHz) [1, 2, 7–9, 12]. To enable wideband FD, recent works [5, 11, 18, 23] have relied on the flexibility of programmable Radio-Frequency Integrated Circuits (RFICs). For example, in our prior work [18], we developed a switched-capacitor delay-line-based programmable IC that has sixteen RF taps, each with independently configurable gain and delay. The large RFIC configuration space, with over 10^{19} possible parameter combinations, offers flexibility at the cost of complexity. An optimal RFIC configuration, computed using a PC (which could take over ten seconds), achieved 23 dB of isolation from the antenna interface and 30 dB of SIC from the RF taps over a 40 MHz bandwidth, as measured using a Vector Network Analyzer [18]. *The RFIC presented in [18] was evaluated using test equipment and it was not integrated into a complete FD radio which would include digital SIC and a Software-Defined Radio (SDR) to transmit and receive actual data.* Accordingly, two important challenges that are under-explored in related works, including [18], are: (i) to design a real-time adaptive controller that enables a highly-complex programmable RFIC to

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achieve and sustain sufficient SIC even when the SI is time-varying; and (ii) to integrate the RFIC (along with its real-time controller) into a complete FD radio that can transmit data over an actual link.

We previously presented two narrowband FD radios within the scope of the Columbia FlexICoN project [24], achieving FD communication across 5 MHz with a single-tap amplitude- and phase-based RF SI canceller [15] and 20 MHz with a two-tap frequency-domain equalization-based RF SI canceller [6]. In this demonstration, we present a wideband FD radio that adaptively controls the RFIC from [18] in real time, achieving 70 dB SIC across a wide bandwidth of 50 MHz through a combination of circulator isolation, analog RFIC cancellation, and digital SIC, reaching the noise floor of the FD radio at −80 dBm. The complete RFIC optimization process is performed in under 1.1 sec, and each fine-tuning adaptation step is performed in under 0.3 sec.

2 DESIGN AND IMPLEMENTATION

Figures 1(a) and 1(b) show the block diagram and implementation of the FD radio, consisting of a circulator-based antenna interface, an RFIC canceller, an FPGA, and a USRP SDR platform controlled from a PC running GNU Radio.

RFIC Canceller. SI at the FD receiver can be very strong, causing nonlinearities at the Low Noise Amplifier (LNA) and clipping at the Analog to Digital Converter (ADC). It is therefore crucial to achieve sufficient SIC directly after the antenna interface. To enable wideband SIC, the RFIC canceller [18] leverages its sixteen RF taps with programmable gains and delays in order to recreate the large SI channel delay spreads with fine resolution. The programmable delays are implemented in a small form factor by means of switched-capacitor delay-lines, ranging from 0.25 ps to 9 ns in steps of 0.25 ps. The programmable gains are implemented using capacitor-stacking and range from 0 to 1 in 6-bit quantization steps.

FPGA platform. The FD radio utilizes a Zynq UltraScale+ MPSoC ZCU104 Evaluation Board [25] to adaptively control the RFIC in real-time. Using a brute force algorithm to search for the optimal RFIC configuration within the $> 10^{19}$ possible gain and delay combinations is impractical. To quickly and adaptively control the RFIC, we implement a closed-loop algorithm with two phases — coarse-tuning and fine-tuning — both of which rely on the offline characterization of the RF taps which are stored in the FPGA's memory. During coarse-tuning, the FPGA employs Orthogonal Matching Pursuit (OMP) [10] with Constrained Linear Least-Squares to select a subset of the RF taps and corresponding configuration that maximizes SIC. In each subsequent fine-tuning step, the FPGA uses Projected Gradient Descent to adjust the gains of the RFIC.

SDR platform. The FD radio employs a USRP-2974 for transmission and reception of OFDM-like data packets [4] encapsulated with Zadoff-Chu pilot symbols for robust synchronization [13]. The SDR and FPGA are both controlled from an Ubuntu 20.04 computer running GNU Radio 3.8 and UHD 4.2 [20, 21]. The custom-made GNU Radio flowgraph estimates the SI channel across the bandwidth of interest [14, 19], and sends it to the FPGA via USB. The FPGA uses the SI channel estimate to search for the optimal RFIC configuration, and then sends the selected configuration to the RFIC canceller via serial communication. Moreover, the flowgraph uses the SI channel estimate to perform digital SIC [6].

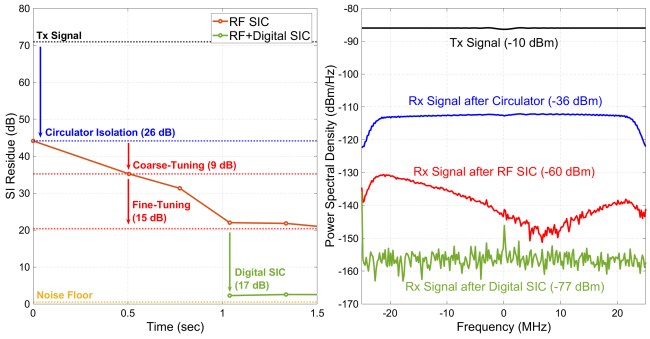

Figure 2: Evolution of the RF and combined RF & digital cancellation over time. The circulator provides 26 dB of isolation. Initial coarse-tuning (0.5 sec) improves SIC by 9 dB. Two fine-tuning steps (2×0.3 sec) add 15 dB, and the total SIC (RF + digital) converges to the noise floor.

3 DEMONSTRATIONS

Experiment 1: Wideband Adaptive FD Radio. This demonstration showcases the capability of the FD radio to quickly achieve and sustain wideband SIC even when the SI is time-varying. In this experiment, the SDR operates at a center frequency of 850 MHz and with a bandwidth of 50 MHz, which lies within the operating frequency of the circulator, and transmits at −10 dBm, which is close to the maximum power admissible by the RFIC [18]. Participants can observe the transmitted and received signals in the time and frequency domains, before and after SIC is applied. In addition, participants visualize the SIC evolution over time, as shown in Figure 2, together with the evolution of the RFIC and digital SIC parameters selected by the optimization algorithms. Furthermore, participants are allowed to modify the environmental conditions near the antenna, requiring the FD radio to adapt quickly. From Figure 2 it can be seen that coarse-tuning takes less than 0.5 sec and fine-tuning less than 0.3 sec. Notice that each of those periods includes packet transmission and reception, SI channel estimation, FPGA computation, and RFIC configuration.

Experiment 2: Throughput Gain of FD Link. In this demonstration, we use two FD radios to establish a wireless link in which both SDRs transmit and receive OFDM-like packets. The center frequency, bandwidth, and power of both SDRs are the same as for Experiment 1. Participants will observe the correct reception of data packets on both FD radios, and measure the improved throughput of the FD link when compared to a Half-Duplex (HD) link. By comparing HD and FD operations, participants will observe that the bit error rate is not degraded due to wideband SIC.

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